Programmable Logic in Mixed Voltage Applications

The use of advanced, deep-submicron IC fabrication processes is resulting in rapidly increasing density and performance for programmable logic devices. However, as device geometries shrink below 0.5 microns, the smallest transistors cannot withstand 5 volts without damage. Thus, the largest and fastest new devices are based on lower supply voltages. For example, the new XC4000XL FPGA family, featuring the industry's highest-capacity, high-performance FPGAs, is based on the 3.3V standard.

To reap the benefits of advanced process technology — including increased performance, increased density, lower power consumption, and lower price — many programmable logic users are making the transition from the 5V standard to lower voltages. This transition affects not only the supply voltage, but also I/O signaling levels. Xilinx is actively taking the lead in working with programmable logic users to plan an orderly transition to a lower voltage standard.

Xilinx introduced the Zero+ product line, the industry's first 3.3V FPGAs, in 1993. Since then, the number of 3.3V product offerings has increased dramatically. However, many other system components remain available in 5V versions only. Thus, mixed-voltage systems employing a mix of 5V and 3.3V components are likely to be the rule rather than the exception in the immediate future.

Xilinx products have been designed with this mixed-voltage environment in mind. 5V input tolerance has been designed into many Xilinx 3.3V devices; these devices accept 5V signals on all I/Os and can drive TTL levels into any 5V device, eliminating all interface issues. Many Xilinx 5V components can directly interface with 3.3V devices. Table 1 lists the Xilinx component product families that can be employed in mixed-voltage systems. All Xilinx device inputs maintain their excellent protection against electrostatic discharge (ESD), even in mixed-voltage applications.

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Mixing 5V and 3.3V Devices

When mixing 3.3V and 5V devices on the same board, I/O signaling levels compatible with both types of components are needed on all signals lines connecting the two types of components. Since both types of supply share a common ground, there are no problems interfacing logic Low levels in either direction, but there are compatibility issues for the logic High levels.

3.3V Devices Driving Inputs on 5V Devices

The lowest output High voltage (V_{OH}) of the 3.3 device must exceed the V_{IH} requirements of the 5V device. Minimum V_{OH} for all Xilinx 3.3V devices is 2.4V, well above the 2.0V minimum High level for TTL signaling. (This includes the XC3000L, XC3100L, and XC4000XL FPGA families and the XC9500 CPLD family when V_{CCIO} = 3.3V.) Thus, all Xilinx 3.3V devices can drive inputs to devices with TTL-compatible input thresholds, including all 5V Xilinx devices. (Note: Some Xilinx 5V devices can be programmed for TTL or CMOS input thresholds; these devices must be configured for TTL-compatible inputs to be directly driven from a 3.3V device.)

5V Devices Driving Inputs on 3.3V Devices

The highest 5V device output voltage must not force excessive current into the input of the 3.3V device. The input structures of Xilinx 3.3V FPGAs include input protection circuits. These protection circuits in the XC3000L and

	Device Family	Accepts 3.3V Compatible Inputs[1]	Drives 3.3V Devices	Key Features
Single Supply V_{CC} = 5V	XC3000A	Yes	With limiting resistor	Low quiescent current
	XC3100A	Yes	With limiting resistor	High performance
	XC4000E/EX	Yes	Yes	Highest density and performance
	XC5200	Yes	With limiting resistor	Cost-effective
	XC9500	Yes	With limiting resistor	5V in-system-programmable, pin locking

	Device Family	Accepts 5V Compatible Inputs	Drives 5V Devices	Key Features
Single Supply V_{CC} = 3.3V	XC3000L	With limiting resistor	Yes	Very low powerdown & quiescent current
	XC3100L	With limiting resistor	Yes	High performance
	XC4000XL	Yes	Yes	Highest density & performance

	Device Family	Accepts 5V Compatible Inputs	Drives 5V Devices	Key Features
Dual Supply				
V_{CC} = 5V				
V_{CCIO}/V_{TT} = 3.3V	XC9500	Yes	Yes	Mixed-voltage system capable

Table 1: *Xilinx products and supply voltage options*

Note: (1) Inputs must be configured for TTL thresholds

XC3100L devices are designed for 3.3V inputs. However, the protection circuits in the XC4000XL devices are designed to withstand 5V levels.

Most 5V devices have complementary CMOS outputs where V_{OH} can reach the 5V rail. (All Xilinx 5V FPGAs and CPLDs, except the XC4000 series devices, have complementary CMOS outputs.) When driving XC3000L and XC3100L inputs (and most other 3.3V devices) from such a 5V device, then the input current must be limited by a series resistor of no less than 150Ω. This guarantees an input current below 10mA, flowing through the ESD input protection diode backwards into the 3.3V supply. That amount of input current is generally considered safe, causing neither metal migration nor latch-up problems. Care must be taken to avoid forcing the nominally 3.3V supply voltage above its 3.6V maximum whenever a large number of active High inputs drive the 3.3V device, potentially causing the 3.3V supply current to reverse direction. The 3.3V V_{CC} power should be on before driving the device inputs from a 5V device.

The I/O structures of the XC4000XL FPGAs have been designed to tolerate being driven to a 5V rail by a low-impedance source. These 3.3V FPGAs can be directly driven by 5V devices with either TTL or CMOS outputs. Power supply sequencing is not a problem; the inputs can be driven to 5V either before or after the 3.3V V_{CC} power is supplied without risking damage to the devices.

In mixed voltage systems, the XC7300 and XC9500 CPLDs can be driven directly by 5V inputs when set up for 3.3V I/O operation (i.e., V_{CCIO} = 3.3V). The input protection diodes in these CPLDs are always connected to the 5V V_{CC} power line, allowing them to tolerate 5V inputs without the need for current-limiting resistors.

If the 5V device has "totem-pole" n-channel-only outputs (as in the XC4000E/EX FPGA series), V_{OH} is reduced by one threshold and the series resistor can be eliminated, provided the nominally 5V supply does not exceed 5.25. Thus, the XC4000E and XC4000EX FPGAs can directly drive any 3.3V device without the need for current-limiting resistors. ◆