GUEST EDITORIAL

HardWire ASIC + LogiCORE = Reduced Time-to-Volume

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Increasingly, systems designers in fast-moving, competitive markets cannot tolerate the long development cycles required for the successful implementation of conventional mask-programmed gate arrays. Successful gate array development time can range from six to 18 months or more, and often requires additional time for re-spins. In addition, the demand for rapid product enhancements has dramatically shrunk typical product life cycles. As a result, leading-edge designers must look for innovative development approaches to reduce risk, while gaining a time-to-market advantage.

As the performance and density of Field-Programmable Gate Arrays (FPGAs) increase, many traditional mask-programmed gate array designers are taking advantage of the fast development time and flexibility of FPGA technology. Submicron CMOS process technology and architectural enhancements are making die sizes more cost-effective; and price points for FPGAs are declining rapidly. In fact, in the lower complexity ranges, FPGAs have been approaching price parity with mask-programmed gate arrays as die sizes in both technologies have become pad-limited.

In the higher complexity ranges, where the cost difference between FPGAs and masked-programmed devices is still significant, the HardWire ASIC model, pioneered by Xilinx in 1989, has gained broad market acceptance. Xilinx FPGA-to-HardWire ASIC migration provides total life-cycle management of high-volume applications by combining the advantages of FPGA development time and flexibility with the cost-efficiency of masked-programmed devices. The technology enables designers to achieve the fastest possible time-to-market and the lowest overall production cost. While the FPGA is in use, late design changes or system upgrades can be accommodated. Production ramps up much more rapidly than it would with a conventional ASIC approach. When the design is final, the systems vendor has the option of requesting a HardWire conversion from Xilinx, leaving no gap between development completion and high-volume production. This represents a major competitive advantage for our users.

> *"Xilinx FPGA-to-HardWire migration provides total life-cycle management of high-volume applications."*

The efficiency of using pre-verified LogiCORE modules for high-complexity FPGA design really brings the HardWire advantage into focus. The system hardware and software verification process can proceed much more rapidly using FPGAs. Concurrent hardware and software engineering is facilitated by virtue of the FPGA, as opposed to the longer development and prototyping time of conventional mask-programmed gate arrays. Hardware corrections, as well as software corrections, can be implemented at the same time, so designers have the option to make optimal corrections, rather than using software patches to work around hardware bugs. The HardWire conversion process preserves the total functionality and performance of the design, including the LogiCORE module.

For example, user-specific PCI designs can be implemented very cost-effectively for high-volume production using the Xilinx PCI LogiCORE module and HardWire ASIC devices. A fully-compliant PCI core and up to 10,000 gates or more of user-specific logic can be implemented for less than $20 in volume quantities.

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Customer re-verification of the complex design is not required with the HardWire solution; Xilinx guarantees equivalent functionality and performance. In some cases (depending on the design), speed improvements can be obtained in the HardWire device by eliminating delays associated with programmable interconnects in the FPGA, and because of the shorter routing delays associated with the smaller HardWire die size.

"HardWire ASIC devices are available to support each Xilinx FPGA family."

About HardWire

HardWire technology allows users to "design once" with FPGAs. It uses FPGA-specific gate arrays and libraries, along with a specialized conversion methodology patented by Xilinx that uses the circuit and physical layout data of the routed and verified FPGA netlist to generate a similar physical mapping of equivalent logic cells in the mask-programmed HardWire device. This ensures circuit equivalence and timing compatibility. Risks associated with design re-targeting and verification are virtually eliminated.

HardWire conversion is superior to conventional gate array conversions because the HardWire conversion is based on "design mapping" at the physical level, rather than common gate array "re-targeting" that begins at the design capture level. Gate array re-targeting actually requires a second complete design cycle after the FPGA development; re-targeting techniques alter the netlist and require significant re-verification effort (and high risk!). The HardWire process reduces the user's expense of time and engineering resources, while offering guaranteed "socket compatibility" and very low risk. Furthermore, the production test program for the HardWire device is developed by Xilinx using a scan path insertion and ATPG (automatic test pattern generation) methodology. No vectors are required from the user and >95% fault coverage of the user's logic is provided.

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