Virtex *Our New Million-Gate 100-MHz FPGA Technology*

Leading process technology, architectural innovation, intellectual property cores, and ASIC design methodology are combined in the new Xilinx Virtex series.

Virtex is the next generation of Xilinx FPGA technology; a new series of high-performance, high-density, system-level devices with a revolutionary new architecture, built with leading 0.25 micron process technology. These FPGAs meet the rapidly growing demand for high-speed system-level functions, helping you create smaller, lower power, more reliable products with more features.

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You can begin Virtex designs today, because Xilinx has been working closely with its EDA partners to provide immediate delivery of the Xilinx Alliance Series software libraries. This development software solution for ASIC designers provides higher performance, faster compile times, and unique innovations that make it much easier to develop very high-density, very high-performance FPGA designs.

The Virtex series, combined with the Xilinx software, represents a new way to approach system-level design.

SelectI/O

The Virtex SelectI/O interface allows a single device to interface with multiple standards simultaneously, eliminating the challenges of multiple signal standards in system design. The Virtex architecture, with its 2.5-volt supply voltage, offers the industry's first devices capable of directly interfacing beyond CMOS and TTL logic. The Virtex series also supports important low-voltage standards such as LVTTL, LVCMOS, GTL+, and SSTL3.

SelectRAM+

The Virtex SelectRAM+ feature allows distributed RAM, block RAM, and high-speed access to external RAM. A common example of system-level designs requiring fast access to varied RAM configurations is a video processing application; where video frame data is stored in megabytes, line data is stored in kilobytes, and pixel and coefficient data is stored in bytes.

For megabytes of storage, the Virtex SelectI/O feature provides 133 MHz external synchronous DRAM access compatible with the SSTL3 I/O standard. Kilobytes of data can be stored in block SelectRAM memory; the Virtex series offers up to 32 blocks of 133-MHz dual-port synchronous SRAM, yielding an internal memory bandwidth of up to 17 gigabytes/second. For bytes of data, Virtex offers distributed SelectRAM memory. Pioneered in the Xilinx XC4000 family, the distributed SelectRAM allows you to create fast and flexible dual-port synchronous SRAMs.

XILINX®

New CLB Architecture

The Virtex architecture is based on logic cells, which are 4-input look-up tables with a register. Each CLB contains four of these logic cells. Each CLB also contains special circuitry for propagating the carry, in addition to special circuitry for implementing efficient multipliers. Combining these features with an abundance of registers makes it very easy to create very high speed, pipelined multipliers for use in DSP and other applications.

Vector-Based Interconnect

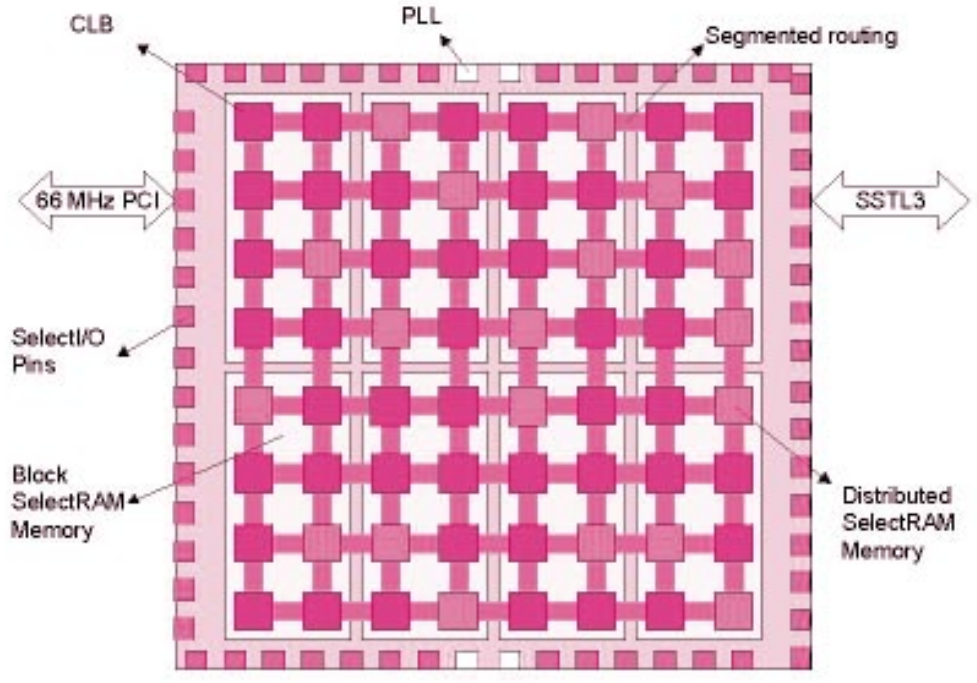
The Virtex series uses a vector-based, variable-length, segmented routing architecture, optimized to allow minimal interconnect delays; this routing is faster and more predictable than that of non-segmented architectures. Vector-based routing results in short, predictable delays that are not sensitive to minor changes in placement. This allows synthesis tools to accurately model interconnect delays in the Virtex Series, without placement information.

Cores

Because it would take many designer-years to create a million-gate system from scratch, Xilinx made the Virtex architecture very adaptable to cores. By optimizing its segmented interconnect capability to create a fundamentally faster architecture, Xilinx reduced the need for architecture-specific cores. Therefore, you can easily implement cores with highly predictable performance using high-level languages.

Availability

The first Virtex device contains 250,000 system gates and 316 user I/O pins. It is expected to be sampling in the second quarter of 1998. Virtex devices that offer up to one million system gates are expected in the second half of 1998. ◆



The new Xilinx Virtex architecture features Xilinx SelectRAM+ memory with distributed and block RAM, plus high-speed access to external RAM via the SSTL3 standard, phase locked loops (PLL), Xilinx SelectI/O pins, Xilinx segmented-routing, and vector-based interconnect.

Figure 1 – *Virtex Functional Block Diagram*