The New XH3 Architecture Combines FPGA and ASIC Technologies

With the new XH3 architecture, Xilinx has combined its FPGA advantages with eight years of HardWire ASIC experience to create the first FPGA-specific ASIC or "FpgASIC."

FpgASICs are true ASIC devices that are designed to meet the performance and feature requirements of Xilinx FPGAs. Both the conversion method, called DesignLock,™ and the device silicon are customized to make the transition from FPGA to ASIC as easy as possible.

The XH3 family has Xilinx-specific FPGA I/Os, JTAG, and control logic built into the base layers of the device. They are exact, pre-verified, ASIC versions of the FPGA features, which are often the most difficult to convert from an FPGA to an ASIC.

For example, the devices have the exact Xilinx FPGA I/O built into the silicon. More than 220 different I/O models have been verified, allowing perfect timing matches for XC4000, XC4000E, XC4000EX, and XC5200 device family conversions.

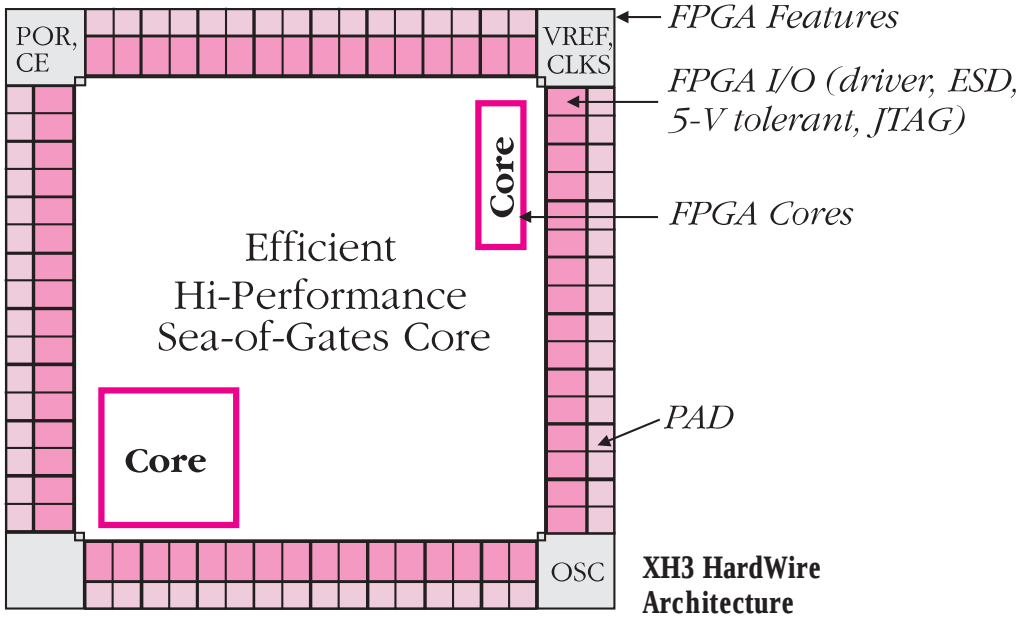
XH3 HardWire ASICs also support Xilinx LogiCORE functions. The PCI macro is completely pre-verified so the transition from FPGA to ASIC is able to encompass tight PCI specifications.

The HardWire DesignLock methodology begins with your completed FPGA files, including the timing, placement and routing information. Throughout the conversion process, these crucial elements are kept intact. The ASIC die are much smaller than the FPGA die, because the programmable elements are replaced with metal vias. However, the relative timing and spatial relationships in the devices are preserved.

As with all conversions, ASIC timing is usually much faster than that of the original FPGA. However, Xilinx tools take all the timing relationships and constraints into consideration so that each path can be precisely verified. Even asynchronous paths can be exactly timed.

The original functionality of the FPGA is preserved throughout the conversion process, eliminating the need for additional vector development. At every step, the conversion process can verify that the original functionality is intact. The Xilinx full-scan methodology generates a complete set of manufacturing fault coverage vectors, with an average fault coverage of over 98%.

XH3 technology is unique in the FPGA/ASIC industry. The HardWire ASIC conversion process now gives you the luxury of designing with FPGAs, while taking full advantage of ASIC cost reductions. ◆



XH3 HardWire Architecture