

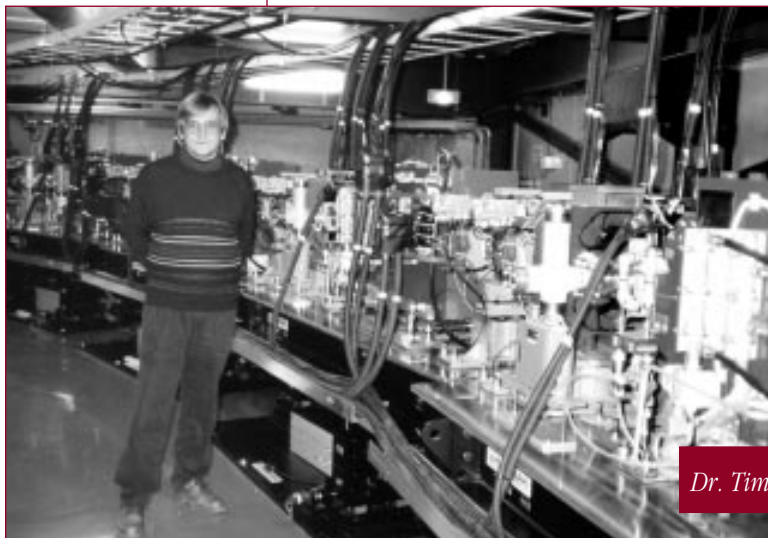
XC3195A FPGAs

Getting a “Handel” on *High Energy Physics*

At the KEK High Energy Physics Accelerator Research Organization in Tsukuba, Japan, Dr. Timo Korhonen has been designing and building a large-scale control system for the Accelerator Test Facility. Instead of using microprocessors for the exacting real-

time processing tasks, he took a novel approach. Dr. Korhonen is using 40 “accelerator cards” from Embedded Solutions, Ltd. (each containing two Xilinx XC3195A FPGAs), and the Handel programming language to generate the hardware configurations for the FPGAs.

The purpose of the project is to build an electron accelerator to evaluate some of the design considerations for a proposed large linear collider. Due to the need for very low beam emittance, the beam path in the 138-metre circumference damping ring must be accurate to a few tens of microns. Thus it is essential to remove even the minuscule deformations of the hall floor that occur due to traffic, construction work, and natural causes such as temperature variations.



Dr. Timo Korhonen in the accelerator test facility

Continued on next page

Continued from previous page

Here is what Dr. Korhonen had to say about his project:

"My part in the project was to design and build a distributed control system to implement dynamic stabilization of the beam path via 36 movable alignment tables that carry the heavy beam steering electromagnets. Positioning of the tables is accomplished by stepper motors with an accuracy of better than 2.5 microns. Laser position sensing is used between neighboring tables to determine the location in each of the five degrees of freedom. This alignment system has never been used before in an operating accelerator.

"I analyzed alternative hardware solutions including microprocessors, microcontrollers, and DSPs; although they were easy to program, Xilinx FPGAs had the edge in performance and could easily interface to my control equipment. I also had to choose the programming tool, and decided to use a radical new programming language, Handel. I saw that this would make the design process much simpler. Besides, it was a good chance for me to get the experience of performing computations in reconfigurable hardware.

"Handel is a programming language designed at Oxford University and now available as a commercial hardware compiler product from Embedded Solutions Ltd. (ESL). It has been designed so that C programmers can rapidly start to build hardware implementations of their programs without having to learn anything about low-level hardware.

"The control system uses up to 40 of ESL's "accelerator" FPGA modules, each containing two XC3195A FPGAs. I used the design methodology that I use normally when writing software. I summarized the data that had to be handled by the system and then refined it top-down to arrive at a software solution. There were a few (really few) hardware aspects that had to be taken into account, such as the specifications for the circuit interfaces which included how to read the ADC, how to handle the RS232 port, and so on.

"This design phase took just a couple of weeks, and the implementation was done in a

"With the ever-increasing capacity and speed of Xilinx FPGAs, I expect them to be used more and more in such applications, and Handel will allow applications to be developed more rapidly and with greater maintainability."

Dr. Korhonen

couple of days using a PC-based system and XACTstep 5.2/6.0. I also have the new Foundation Series software but haven't yet upgraded to it. After working a few days with Handel, the feeling was just like writing software and at times made me forget that what I was doing was actually hardware development. Recently, I implemented a digital module with more traditional methods and the difference in productivity was really overwhelming.

"The next big challenge will be in applications that need fast real-time I/O; for example, reading the data from beam monitors, processing it, and feeding the results directly back to a control system. This is a task where even the fastest available CPUs find difficulty because the data has to go through the I/O interface. In an FPGA-based system, most of the overhead can be avoided, and thus the response time is shortened. For these tasks, I'll probably use the Xilinx XC4000XV devices."

For more information:

Dr. Timo Korhonen:

timo.korhonen@kek.jp

Embedded Solutions Ltd.

(Handel and Accelerator Cards):

sales@embedded-solutions.ltd.uk

<http://www.embedded-solutions.ltd.uk/>

Oxford Hardware Compilation Group:

<http://www.comlab.ox.ac.uk>

[/oucl/hwcomp.html](http://www.comlab.ox.ac.uk/oucl/hwcomp.html) ◆