Designing with the Spartan Series FPGAs

by MARC BAKER

The new Xilinx Spartan Series has already met with great success in high-volume FPGA applications of up to 40,000 system gates. All five 5-V versions are in full production, including a new -4 speed grade that provides the fastest 5-V FPGA in the industry. And, the 3.3-V Spartan-XL devices are on schedule for introduction in the third quarter.

A key benefit of the Spartan Series is the complete software solution. Software support was available even before the devices were introduced, and the same will be true of the 3.3-V versions. You can get started with Spartan designs immediately, knowing that you can take advantage of today's 5-V devices, or tomorrow's even-lower-cost 3.3-V devices.

Design Entry Support

Because the Spartan Series is based on our highly acclaimed XC4000 family architecture, any design entry tool that supports the XC4000E family can be used for the Spartan Series. For schematic capture tools, select the XC4000E library. This library is used automatically when the Spartan family is selected in the Xilinx Foundation Series software. The only XC4000E library components that are not allowed in the Spartan architecture are the edge decoders (DECODE*x*), wired-AND gates (WAND*x*), mode pins, (MD*x*), and asynchronous RAM (RAM16X1, RAM32X1). The Spartan architecture supports both single-port and dual-port synchronous RAM, which have S and D suffixes, respectively. If you accidentally use an unsupported component, the Design Rule Checker will notify you.

FPGA synthesis tool vendors have spent the last few years optimizing their algorithms for our highly successful XC4000 Series architecture. The Spartan Series immediately takes advantage of that development effort, achieving excellent synthesis results from multiple tool vendors. Support is available today from Synopsys, Exemplar, and Synplicity.

Core solutions targeted to the Spartan Series shorten time-to-market by providing a pre-verified solution. The faster speed grade allows Xilinx to offer the 32-bit, 33 MHz LogiCORE PCI interface for the XCS30-4. The upcoming Spartan-XL family will extend that support to 3.3-V solutions. All Xilinx DSP LogiCORE solutions also support the Spartan Series, making FPGAs even more cost-effective for digital signal processing.

Xilinx AllianceCORE partners have been updating and verifying their solutions in the Spartan architecture:

- **CoreEl Microsystems** has introduced Asynchronous Transfer Mode (ATM) products for the XCS30-4 device.
- **Integrated Silicon Systems** has added a Reed-Solomon Decoder for the XCS40-3 device, in addition to their existing Encoder for the XCS10-3.
- **Memec Design Services** offers an industry-standard 8250 core for the XCS05-3.
- **Virtual IP Group** offers five different cores for the XCS40-3, including several UART and 82XX peripheral functions.
- **CAST, Inc**. offers a Viterbi Decoder and a C2910 Microprogram Controller.

Design Implementation Support

The Xilinx Alliance Series and Foundation Series software 1.4 supports implementation of all Spartan 5-V devices. The cost of the complete Spartan software solution is reduced by making all five device densities available in the Base (lower cost) development system.

At the time of the 1.4 software release, the Spartan -4 speed file was not yet available, so it must be downloaded from WebLINX, our web site:

www.xilinx.com
/techdocs/htm_index/sw_speed_files.htm

The -4 speed file on the 1.4 CD is only a placeholder and should not be used to estimate Spartan performance. The complete -3 and -4 speed grade numbers are available in the latest Spartan data sheet on WebLINX:

www.xilinx.com
/partinfo/ds060.pdf

The Spartan Series offers an optimized pinout for the 208-pin Plastic Quad Flat Pack, providing nine more I/O pins and eight more Vcc pins to enhance I/O switching characteristics. The package file must be downloaded from:

www.xilinx.com
/techdocs/htm_index/sw_package.htm

Additional device files available for download include the IBIS models of the I/O structures, useful for board-level simulation:

www.xilinx.com
/techdocs/htm_index/sw_ibis.htm

Boundary Scan Description Language (BSDL) files allow you to take advantage of the built-in IEEE 1149.1 JTAG test capability:

www.xilinx.com
/techdocs/htm_index/sw_bsdl.htm

Designing for the Upcoming Spartan-XL Family

The 3.3-V version of the Spartan architecture will not only bring the Spartan family benefits to 3.3-V applications, but also further reduce the cost for high-volume applications. Prototyping can begin today in anticipation of the silicon introduction in the third quarter of 1998.

If a 5-V power supply is available in the prototype system, use the corresponding 5-V Spartan device as the prototype. The Spartan-XL architecture will be compatible, although timing specifications will differ. You should re-run the design with the Spartan-XL speed files when available.

If the prototype must be a 3.3-V device, the XC4000XL family can be used until the Spartan-XL device is available. Because the XC4000XL architecture is different, you should still implement the design in the target Spartan device first to verify the fit. Once the design fits into the Spartan architecture, lock down the I/O pins and re-implement using the XC4000XL prototype. *See the Spartan/XC4000XL Compatibility chart on page 28.*

Choose an XC4000XL device with an equivalent CLB count to the target Spartan device. The XCS05XL has no equivalent, so use the larger XC4005XL. If the CLB count is sufficient, all other resources will also be sufficient. The design should avoid the PQ208 package, where the XC4000XL prototype would not be able to match the Spartan pinout. The XC4000XL packages also do not offer equivalents to the XCS20/30VQ100. All other Spartan packages have equivalents in the XC4000XL family.

You will need to re-verify the timing once the Spartan-XL speed files are available. To ensure that the Spartan-XL -4 speed will be sufficient, verify the design using the XC4000XL-2 speed grade. The Spartan-XL -4 speed is expected to be at least one speed grade faster than the XC4000XL-2, but using the -2 as a prototype compensates for potential variations in routing and final timing parameters.

The XC4000XL prototype must use one of the two Spartan serial configuration modes, which are selected as all zeroes or all ones on the three mode pins. The Spartan pinout has only one mode pin, equivalent to M0 on the XC4000XL device. To easily adapt the board to the Spartan device, use removable resistors or jumpers on the three XC4000XL mode pins, and simply remove the two jumpers on M1 and M2 when substituting the Spartan-XL device.

Summary

Because we based the Spartan Series architecture on the highly successful XC4000 series, we not only provide excellent devices, but we also provide strong, proven, software support for the family. Designs can be completed today using the production Xilinx development system and a wide variety of third-party tools. You can find the latest information on the Spartan Series and its software support on www.xilinx.com/

Using the XC4000XL for prototypes, and the lower cost Spartan-XL for production.

SPARTAN-XL/XC4000XL COMPATIBILITY CHART						
Spartan-XL (Production) Speed Grades -3,-4			**XC4000XL (Prototype)** Speed Grades -3,-2			
Part No.	**Total CLBs**	**Usable I/O**	**Part No.**	**Total CLBs**	**Usable I/O**	**Common Package**
XCS05XL	100	61	**XC4005XL**	196	61	PC84
		77			77	VQ100
XCS10XL	196	61	**XC4005XL**	196	61	PC84
		77			77	VQ100
		112			112	TQ144
XCS20XL	400	113	**XC4010XL**	400	113	TQ144
XCS30XL	576	192	**XC4013XL**	576	192	PQ240
		192			192	BG256
		113			113	TQ144 (HT144[2])
XCS40XL	784	193	**XC4020XL**	784	193	PQ240
		205			205	BG256
Speed	-3		**-3**			
Grade	-4		-2			

See article on page 5