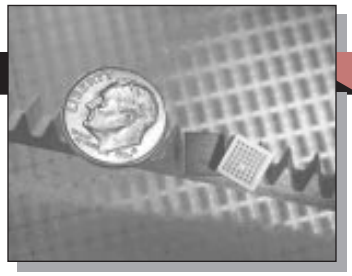

NEW

Chip-Scale Packaging:

Ideally Suited to Today's Portable and Small Form-Factor Applications

by Frank Toth, Marketing Manager for FastFLASH Products, toth@xilinx.com

Xilinx recently unveiled a new 48-lead chip-scale package (CSP) that offers all the benefits of an extremely small form factor in a rugged ball grid array package. This package is ideally suited for a growing number of applications where minimal board space and package thickness are important, such as portable and wireless designs, PCMCIA cards, PC boards, and PC add-in cards. Xilinx is the first non-memory manufacturer to have chip-scale packaging (CSP) technology available now.

Chip-scale packages are about 20% larger than the size of the die, with a ball pitch less than one millimeter. With these packages, the requirements for handling and lead coplanarity are greatly reduced because there are no fragile leads to bend. The package is also very thin (1.3 to 1.8mm) and light weight (0.17 gram) which makes it ideally suited for weight conscious portable applications like cell phones, hand held inventory and bar code reader systems, and personal digital assistants.

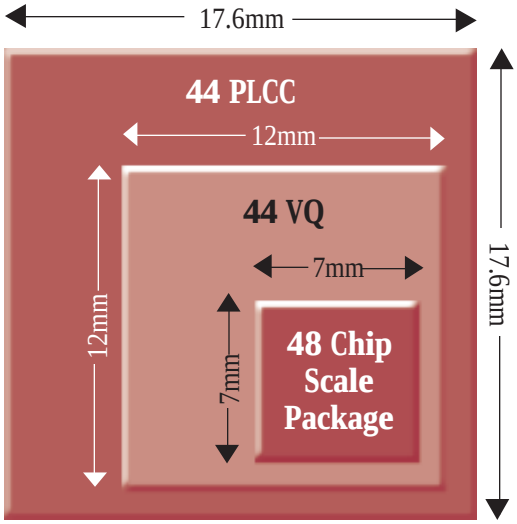

Figure 2

Figure 1 shows a side view of how the package is constructed. The die is mounted on top, bonded to the substrate surface, and wire bonded using industry-standard techniques. Thermal resistance of the package (Θ_{JA}) is 45.5°C per watt, which is comparable to the VQ44 package at about 42°C per watt. System manufacturers using CSPs can benefit from CPLD speed and cost improvements (die shrinks) without ever having to change package footprint, because die shrinks can be accommodated without having to change package dimensions.

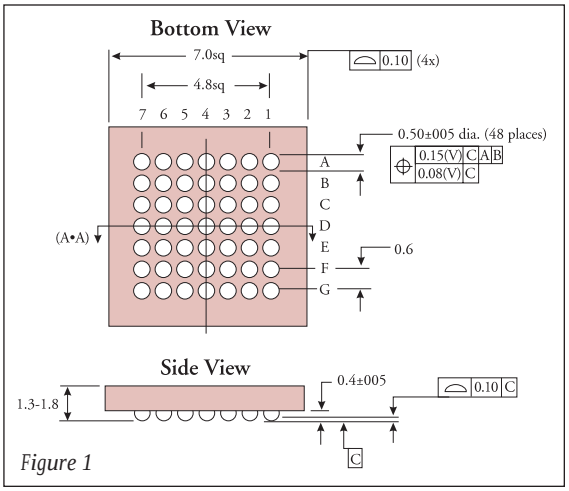

Figure 1

The XC9536 is the first XC9500 FastFLASH ISP family device offered in this package. It features 34 I/Os, full IEEE 1149.1 JTAG support, 10,000 program/erase cycles, 20 years of data retention, and unmatched logic flexibility with the industry's best CPLD pin-locking. The XC9536 CSP has 48 pins arranged in a seven-millimeter by seven-millimeter configuration using a 0.8 millimeter solder ball pitch. (Package technologies with a ball pitch greater than 0.8 millimeters are considered ball grid arrays and not CSP.) The footprint is three times smaller than the 44-pin very thin quad (TQ44) package and 40 percent smaller than the 48-pin thin quad (TQ48) package, as shown in **Figure 2**.

For more information on chip-scale packaging, visit WebLINX at: www.xilinx.com/products/csp.htm ◆

XILINX®