New Spartan -4 Devices for High-Speed Applications

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The low-cost Spartan FPGA family is excellent for high-volume consumer applications such as PCs, digital cameras, set-top boxes, and DVD equipment. Now, with the introduction of the new Spartan -4 speed grade, the family can be used in very high-performance applications as well, delivering on the promise of being the industry's no-compromise ASIC-replacement FPGAs.

For example, the two largest Spartan devices can now meet the stringent requirements of 33 MHz PCI applications with no wait states, making this the first low-cost FPGA family to provide such high performance, with many applications running at beyond 80 MHz.

Last year, 76% of ASIC design starts required 80 MHz speed or less. With an I/O speed beyond 100 MHz for the smaller members of the family, and internal frequencies that can go much higher, the Spartan devices easily meet this requirement.

Spartan –4 Performance

The new Spartan -4 speed grade is approximately 25% faster than the original Spartan -3. This makes it comparable to the XC4000E-1, and faster than any competitor's 5V FPGAs. I/O frequency is commonly used as a performance benchmark, because it indicates how fast two devices can "talk" with each other. I/O frequency is measured by taking the inverse of the pin-to-pin clock-to-out and setup delays. The Spartan -4 excels in this respect, with an I/O frequency of 92 MHz for the XCS30; this is 12% faster than the comparable XC4013E-1, at 82 MHz. For the two smaller Spartan devices, the XCS05 and XCS10, the I/O frequency surpasses 100 MHz *(see **Figure 1**)*.

Spartan is a full-featured family with on-chip SelectRAM memory and 238 to 1836 logic cells (5K to 40K system gates). It takes advantage of a unique process that utilizes 0.5 micron technology for transistors and 0.35 micron technology for interconnect. This provides the smallest and fastest logic, using a 5V supply.

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Spartan –4 Speed Files

The -4 speed files were generated with a new characterization methodology that more accurately models the worst-case delays in the silicon while reducing the test cost. The result is a very fast, yet low-cost solution. By applying this new methodology to the volume production units now being processed for the Spartan family, the Spartan -3 speed grade was simplified and overall performance was improved as well.

To use the new –4 speed grade, download the speed files from WebLINX, the Xilinx website

The initial Spartan support in the Xilinx software (Alliance Series and Foundation Series version 1.4) includes a placeholder for the -4 speed files, making it easy to drop in the new files; installation instructions are included in the "readme" file. The production versions of the Xilinx Alliance Series and Foundation Series version 1.5 software will include the new speed files. If you are using the beta version of the 1.5 release, make sure you have the correct speed files.

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Spartan Speed Designator

The Spartan series uses a new speed designator that starts at an arbitrary number and increases for higher speed. Thus, the Spartan -4 is faster than the Spartan -3, but the "-4" doesn't indicate any relative speed against other products. All future Xilinx products will use this new nomenclature, which is similar to speed designators in the ASIC world. This avoids the problems of having two-digit speed grades. It also avoids the potential for basing performance assumptions on a single specification.

For example, most Xilinx devices use the delay through the Look-Up Table (LUT) for the speed designation. The Spartan -4 has a 1.2 ns LUT delay, the fastest of any Xilinx 5-volt FPGA, equal to the XC4000XL-09 and faster than the XC4000E-1 (1.3 ns). However, the Spartan -4 overall performance is typically slower than the XC4000XL-09, and comparable to the XC4000E-1 *(see **Figure 2**)*.

The lookup table delay, being just one small part of any given path in a design, does not accurately reflect overall performance, and does not work well as a general method of comparing speeds. Overall design speed depends on the function being implemented and the routing delays in the critical path. Those routing delays can be as short as 0 ns, especially when using carry logic. As an example, a 16-bit counter runs at 96 MHz in the XCS30-4. The Xilinx Timing Analyzer and third-party simulation tools will report worst-case delays with a 0.1 ns resolution.

Spartan Core Support

The new Xilinx PCI32 Spartan master and slave interface further reduces the cost of implementing a programmable PCI solution (*see the related article on p 14)*. Xilinx also offers several DSP-related cores for the Spartan architecture, along with AllianceCORE solutions from other vendors. All of these pre-defined solutions can immediately take advantage of the higher speed offered by the Spartan -4 speed files. Download the new files today to take advantage of the fastest low-cost FPGAs available.

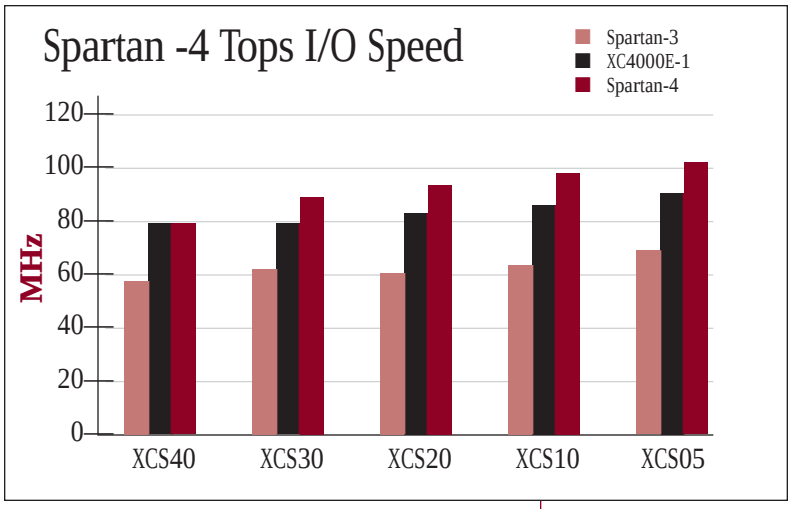

Figure 1

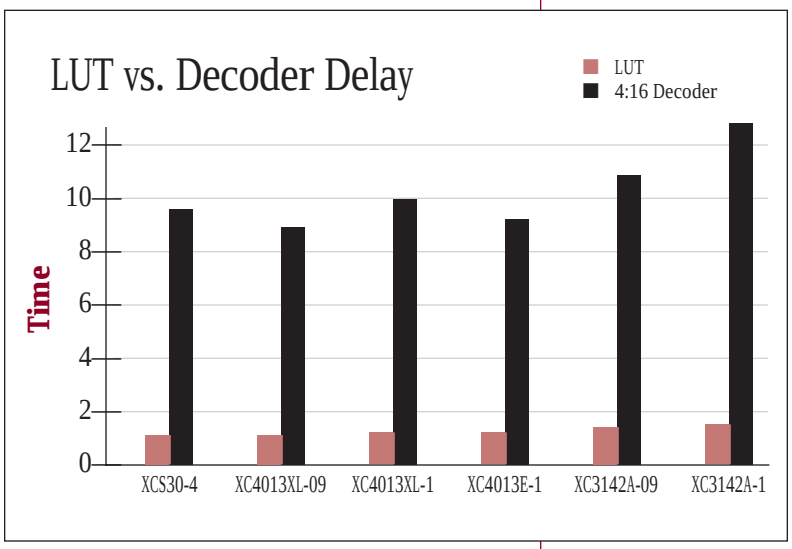

Figure 2

You can download the latest datasheet from WebLINX at http://www.xilinx.com/partinfo/spartan.pdf. Note that as with all other Xilinx FPGAs, the datasheet provides the guaranteed worst-case pin-to-pin setup and hold times, which are not reflected in the speed files or timing reports.

Spartan –4 devices are available on distributor shelves today, for all densities and packages. ***Contact your local salesperson or distributor for pricing and lead-times.*** ◆