## How does the EXTEST instruction work in the XC4000/XC5200 series devices?

The XC4000 and XC5200 series devices implement the *IEEE 1149.1*-compatible EXTEST instruction. Loading a bit sequence "000" in the Boundary Scan Instruction register (IR) will enable the EXTEST instruction.

**Figure 1** shows the Boundary Scan Logic in a typical IOB. The Boundary Scan Data register (DR) is a serial shift register implemented in the IOBs. Each IOB can be configured as an independently controlled bi-directional pin. Therefore, three data register bits are provided per IOB: for input data, output data, and 3-state control.

An update latch accompanies each bit of the DR, and is used to hold test data during shifting of new test data. The update latches get updated during the *Update-DR* State of the TAP controller.

To execute the EXTEST instruction, shift the bit pattern "000" into the IR in the *Shift-IR* state of the TAP controller via the TDI pin. This instruction will become current in the Update-IR State and the EXTEST line will get asserted. At this time, data in the input bit of the DR gets driven on to the FPGA interconnect (IOB.I) and data in the output and 3-state control bits gets driven to the device pins.

In the *Capture-DR* State of the TAP controller, data from the device pins goes to the DR input bit (Shift/Capture line de-asserted); it gets captured in the IOB flip-flops. Care should be taken to make sure that the output bit of the DR has been 3-stated at this point, otherwise there will be contention on the pin and unknown data will get captured. The output and 3-state bits of the DR capture the data coming from the FPGA interconnect in this state (IOB.O and IOB.T).

This captured data can be shifted out for inspection on the TDO pin during the *Shift-DR* State of the TAP controller (Shift/Capture line asserted).

**Note 1:** The *IEEE* standard *1149.1* does not require an internal injection of data to the device interconnect during the *Update-IR* state. However, this capability helps to compensate for the lack of INTEST support.

**Note 2:** The Update latches are accessed every time the TAP controller is in the *Update-DR* state, regardless of the instruction. Care must be taken to ensure that appropriate data is contained in the update latches prior to initiating an EXTEST instruction. Any instruction, including BYPASS, that is executed after the test data has been loaded, but before the EXTEST instruction becomes current, changes the test data. ◆

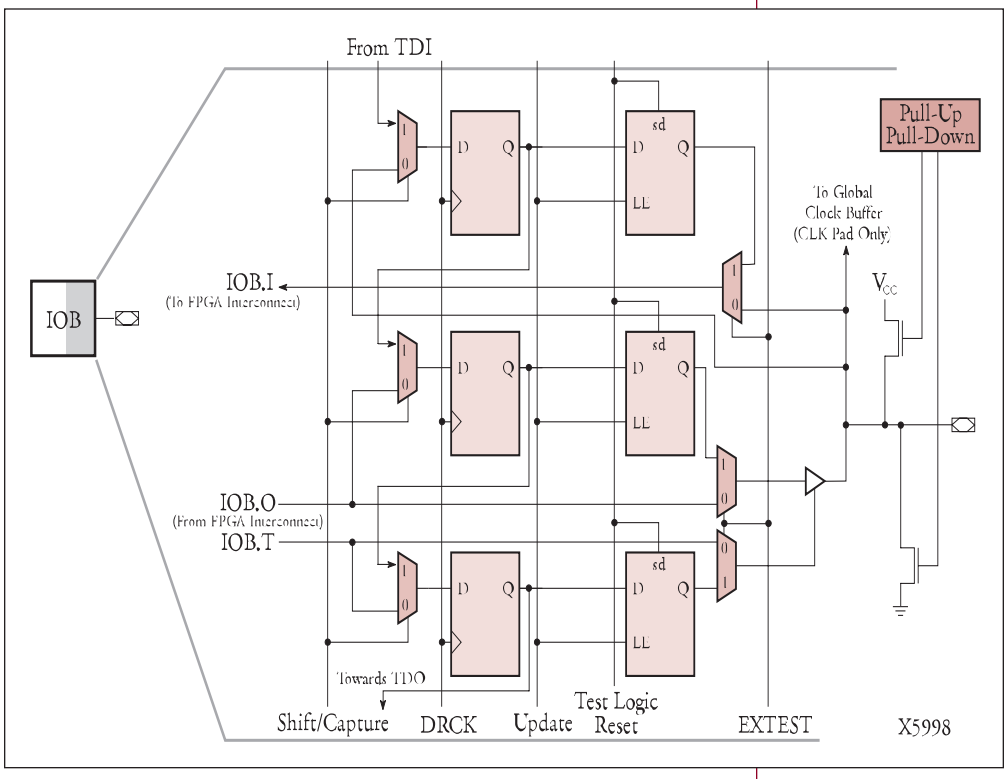


*Figure 1 – Boundary Scan Logic*