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The Rapidly Changing ASIC Conversion Market

As programmable logic devices continue to grow in density, designers are increasingly using FPGAs where they previously used ASICs. The advantages of off-the-shelf availability and rapid prototyping make FPGAs a very attractive solution. However, you must answer a key question: will you use FPGAs for both development *and* production volumes, or will you convert the design to some form of ASIC, such as a gate array or standard cell, for cost reduction?

Third-Party ASIC Conversion Problems

The FPGA-to-ASIC conversion market has been dynamic over the past few years. Several companies have entered the market, only to find themselves in financial trouble. Microchip Technologies exited after 15 months of business and the D.I.I. group who purchased Orbit Semiconductor took a $60M loss last quarter due to the difficulties they continue to experience. It is not due to a lack of conversion business in the marketplace that problems are caused for the small ASIC vendor. The problem is caused instead by the difficulty of accurately converting today's complex PLDs. There are several factors contributing to this.

"Will you use FPGAs for both development and production volumes, or will you convert the design to some form of ASIC, such as a gate array or standard cell, for cost reduction?"

Most third party FPGA-to-ASIC conversion companies use gate array technology for the translation. The features of today's FPGAs, such as PCI compliance and the ability to implement 50K bits of RAM or more, exceeds the capability of most gate array vendors. In addition, the growing requirement for fast, on-chip RAM is perfectly suited to SRAM-based FPGAs, or fully diffused standard cell embedded RAM, but not for gate array processes. Even the most efficient gate array process will require 5 to 6 gates per RAM bit to convert FPGA RAM to ASIC RAM. For a design with 15K bits of RAM, this can translate into a minimum of 90K gates on a gate array. Therefore, a design that was slated for cost reduction from an FPGA to a smaller gate array may achieve only a small cost reduction because of the increase in die area required for the RAM.

Gate array price erosion has been fierce in the past few years. While this price reduction has benefited companies using gate arrays, some of the smaller gate array vendors are in poor financial condition, making it difficult for those companies to sustain innovation. This lack of new product development is now causing them to have difficulty converting many of the more complex FPGA designs.

Leaving an FPGA conversion to a third party gate array company is complicated, not well suited technologically, and doesn't offer much cost reduction because a 100K-gate FPGA often becomes a 500K gate array under these circumstances.

Pad Limitation

True pad limitation is achieved when there is such an abundance of gates available in a device, that the size of the die is determined solely by the number of required pads. The standard cell providers, with their dense core offerings, have been pad limited for some time. At process geometries below 0.5µ, many architectures, including FPGAs and gate arrays, become pad limited. For an FPGA-to-ASIC conversion company, who depends on achieving cost reduction through a die area shrink, pad limitation reduces the cost benefit of the gate array. In many cases, because the customer needs all the pads provided on the FPGA, the gate array device will be of equal size, in order to include the same number of pads. Size reduction due to translating programmable SRAM gates to much smaller metal vias is nullified.

Diverging Architectures

While the features and performance of FPGAs continually increase to include many ASIC-like features, the actual implementation and design methodology are becoming dissimilar; architectur-

ally, FPGA technology and ASIC technology are diverging. The ability of one architecture to be "converted" to the other will require more than just re-targeting to a specific ASIC vendor's libraries. Gate array processes without embedded RAM structures that are specific to the original FPGA will quickly exceed gate count capability. In addition, in-depth knowledge of the FPGA's functionality and detailed specifications of industry standards like PCI will be basic requirements. Furthermore, the ability to provide accurate timing of I/Os and critical system performance will be essential to convert these newer, more complex designs.

FPGA designers who depend on ASIC cost reductions will find their options changing over the next 18 months. Many smaller ASIC vendors will de-emphasize FPGA conversions because they lack the capability to convert them in a cost-efficient and technically effective manner. In the meantime, FPGA price per gate continues to decline to a point that, for 40K system gates and below, FPGAs can be considered for production volume in "formerly ASIC" applications. Companies that continue to provide FPGA-to-ASIC conversions will need to offer increasingly FPGA-specific solutions, because a generic gate array process will not serve the requirements of all PLD features.

Xilinx is one example of a company that provides a specialized solution for FPGA conversions. The Xilinx HardWire Business Unit continues to develop new ASIC technologies suitable for converting complex, RAM-intensive FPGAs. Xilinx recently introduced the XH3 FpgASIC architecture which provides dense gate array logic surrounded by an I/O ring that replicates the Xilinx FPGA I/O. FPGA features are built into the base arrays, further reducing the risk of conversion problems.

Xilinx HardWire devices are an excellent cost reduction path for FPGA's above 40K system gates and are especially suited for most dense FPGAs.

Another company specializing is Clear Logic Corporation, who offers a solution for Altera FPGAs only. Clear Logic offers their proprietary ClearFire ™ technique for laser cutting metal fuses in base arrays which closely resemble the logic resources in the Altera Flex8000 family of FPGAs. The advantage to the customer is that by optimizing processes, libraries, and feature sets to convert Altera PLDs exclusively, the risk of converting the design incorrectly is reduced. In the future, this type of focus will be required to provide accurate FPGA cost reductions.

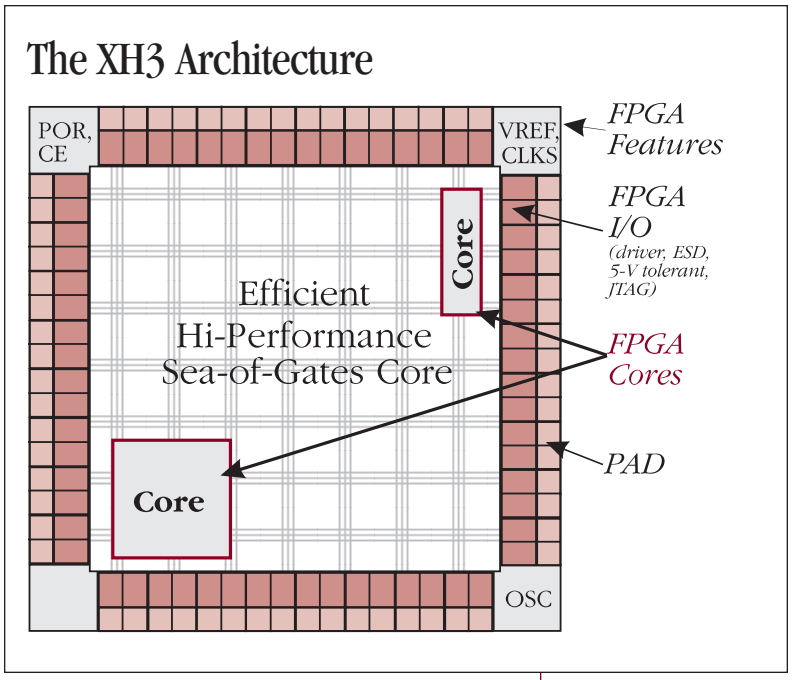

Figure 1: XH3 Architecture

Conclusion

In the future, FPGA technology will be increasingly suited for applications previously considered as gate array or standard cell territory. Many logic designers are realizing that they can take advantage of FPGA time-to-market benefits and still achieve a gate array cost point for volume production.

However, options for translating the FPGA to an ASIC are changing. Because of the complexity of the FPGA features and the density of RAM, many smaller gate array conversion vendors are dropping out of the market. Pad limitation for both FPGA's and gate arrays can minimize cost reduction benefits unless creative pad options can be implemented. Architecturally, FPGA's and gate arrays are also diverging. Differing design methodology and RAM implementations can be very inefficient if not specifically accounted for in the conversion process. The new models for success in the conversion market will be companies who specialize in converting a single architecture, such as Clear Logic with Altera devices, Lucent with MACO™ and Xilinx with HardWire FpgASIC's. These will be the options that provide the closest match and the most expertise for the 200K+ gate FPGA's of today.