FROM THE EDITOR

EDITOR
Carlis Collins
editor@xilinx.com
408-879-4519

SENIOR DESIGNER
Jack Farage

BOARD OF ADVISORS
Dave Stieg, Dave Galli
Mike Seither, Peter Alfke

PUBLICATION SERVICES
Ruddle Creative
111 N. Market St., Suite 715
San Jose, CA 95113
Tel: 408-297-3000 or
1-800-7RUDDLE
Web: www.ruddle.com

XCell

Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124-3450
Tel: 408-559-7778
Fax: 408-879-4780

Imagination Springs to Life...

Each new generation of programmable logic technology moves us one step closer to the ideal development environment, and the new million-gate Virtex FPGAs and development tools from Xilinx are a quantum leap forward. This new creative technology, a combination of both device and software breakthroughs, is an extraordinary advancement that can dramatically increase your productivity and help quickly bring your new creations to life. This issue of Xcell will show you some of the creative possibilities offered by the new Virtex family.

Programmable logic technology is the most direct link between your imagination and the physical world of digital systems. When this link works quickly and efficiently, you are free to explore your creative genius; your ideas can flow smoothly into new, unexplored territories, unimpeded by the often slow and mundane chores of design implementation. The total Virtex solution is a combination of advanced new technologies, including device architecture, development software, and highly efficient manufacturing processes that work in harmony to give you an ideal development environment. *There is no faster or less expensive way to get your creations into full high-volume production.*

The Virtex architecture is revolutionary, with many new system-level features that make it much easier for you to put an entire system on a single device. It was designed from the beginning to work efficiently with the High-level Description Languages, cores, and advanced software algorithms that are available today, making it much easier for the software to implement your designs. This gives you the highest system performance, in the highest-density FPGAs ever produced, with compile speeds of over 200K gates per hour – a 4X runtime improvement over previous solutions.

The Virtex runtime performance breakthroughs are due, in part, to a very flexible and predictable routing structure that works closely with our latest place and route algorithms. Plus, the new Virtex library is optimized for the Virtex architecture, taking full advantage of its unprecedented capabilities. Simulation and compile times have also been reduced because the netlist is 40% smaller, making your designs easier to debug while also consuming less disk space.

The Virtex architecture is compatible with ASIC-like RTL coding styles. This means that if you are new to HDL, you will have a reduced learning curve and achieve higher design speeds using "generic" coding styles. The vector-based interconnect structure also gives you a more accurate post-synthesis timing estimation. This allows you to spend more time designing with the front-end synthesis and RTL verification tools and less time dealing with the back-end implementation tools.

To help you get a better understanding of the many new creative possibilities that are now available to you, we have included an abbreviated Virtex family data sheet in this issue, starting on page 41. For the complete data sheet and application notes, visit: www.xilinx.com/products/virtex.htm

Thanks for reading Xcell. What do you think of the new format? E-mail your comments to editor@xilinx.com.