Integrate FPGA & System Design Using Concept® HDL

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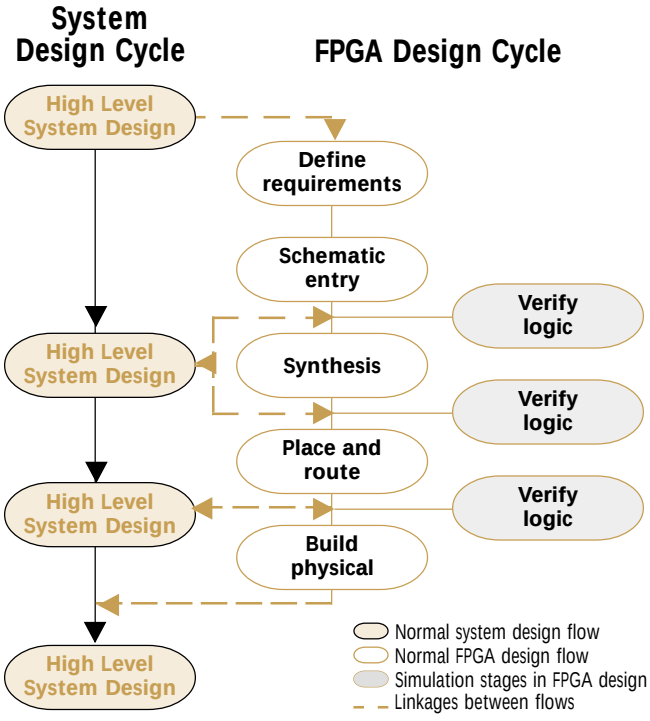
Concept HDL from Cadence Design Systems takes a big step forward in integrating System and FPGA design cycles. The latest release of Concept HDL (PE 13.5) provides many new features for FPGA design, including the capability to concurrently design the FPGA and the system that uses it.

Concept HDL has come a long way from the times when schematic entry was limited to adding gate-level primitives from FPGA vendor libraries. Now it supports top-down, mixed-level, and bottom-up FPGA design flows. From the system design perspective, Concept HDL provides a framework that seamlessly integrates FPGA and board design cycles. FPGA designers can use all Concept HDL features already available to the system designers. They can use Global Find, Global Navigate, Hierarchy Editor, and design reuse capabilities in addition to the features of earlier releases. This article focuses on how this high level of integration between the Concept HDL-based board design flow and FPGA flow can benefit you.

The Integrated Flow diagram shows the system design phases and their integration with the FPGA design phases. This article illustrates this flow using the example of an image-processing card based on a Xilinx FPGA for use with a general-purpose microprocessor-based computer.

Integrated FPGA and Board Design Flow



High Level System Simulation

Concept HDL, based on the HDL-centric data model, provides the power of the HDL-based methodology with the convenience of schematic-based design. While designing an FPGA as a part of a system, you may initially simulate the system using its behavioral model to refine the expected behavior of the FPGA. This feature is especially useful for systems with many FPGAs. You can use different simulation models for the same component. You may simulate your designs using a combination of Verilog®, VHDL, smart models, and Hardware models. The HDL-centric architecture also provides for easy third-party tool integration and a high level of integration with simulators like Verilog-XL simulator, Affirma™ Native Compiled Verilog™ simulator, Leapfrog® VHDL simulator, and Affirma® Native Compiled VHDL simulator. You can also cross-probe the HDL code from Concept HDL — a valuable aid for debugging.

The facility to mix and match different types of simulation models provides a greater degree of design freedom. You can refine the expected behavior of the FPGA through these high level simulations and use this model to drive the FPGA design. The test vectors developed here can be used through the design cycle.

For the image processing card example, you may verify the image processing interfaces and algorithms by simulating a behavioral FPGA model with simulation models of the microprocessor, memory elements, and other system components. Thus, Concept HDL's powerful simulation capabilities allow you to refine the FPGA requirements very early in the design cycle using top-down synthesis and design of blocks

You can either directly synthesize the behavioral description of the FPGA using Synplify or design the FPGA using Concept HDL's extensive design capabilities. Concept HDL is fully integrated with Synplify from Synplicity for design synthesis so that you can specify Synplify synthesis attributes that drive and control synthesis, directly on the schematic blocks. Concept HDL automatically passes the synthesized structural netlist from Synplify to the Xilinx place and route tools.

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Alternatively, you can create a complete design for the FPGA in Concept HDL. You can even choose to synthesize only parts of the design. This design can be flat or hierarchical, based on your preferences. Concept HDL helps you quickly create schematics from symbols or create symbols from schematics, and ensure consistent interfaces between different views. Concept HDL's design reuse features allow you to reuse older designs and save valuable design time. Concept HDL's simulation framework also allows you to simulate the FPGA block separately or simulate just some parts of it. You can easily simulate and compare the pre- and post-synthesis simulation results to verify the synthesis.

For the image processing example, you can reuse multipliers designed earlier, and synthesize only the control logic. Thus, the full integration with simulation helps you verify the functionality at any stage of the design. Concept HDL's extensive features and flexibility coupled to the integration with Synplify help you design and verify complex FPGAs with ease.

Smooth Flow with Xilinx Place and Route Tools

Once you complete the logic design for the FPGA block, you can pass the design to the Xilinx place and route tools by just clicking a few buttons. You can also directly invoke the Xilinx Design Manager from the Cadence Programmable IC flow.

After your FPGA design is complete, using the Xilinx Alliance Series software, you can do post-route simulations using the post-route HDL files and timing data. SDF back annotation and simulation features let you compare simulation results among the behavioral model, logic-level FPGA design, and post-route FPGA design. The Concept HDL framework allows you to use the same test vectors for different views of the design (pre-route, post-route) making the comparison easier. Thus you can verify that the FPGA meets design requirements after including all physical delays.

Concept HDL's framework allows you to verify the correctness of your designs at various levels of abstraction, at different stages of your design cycle, with minimal effort.

Easy Transfer of Data Between FPGA and PCB Tools

After your FPGA design is complete, you can automatically create a view for Allegro®, Cadence's benchmark PCB design tool. The normally tedious process, to ensure correct integration for system-level simulation and PCB design, is fully automatic, saving valuable design effort. This ensures that it is very easy to incorporate engineering changes. It is also possible to specify properties and constraints to guide the PCB tool on the FPGA design itself. The painless and reliable transfer of FPGA design information to the PCB design solution is a key feature of the Concept HDL design flow.

Managing Signal Integrity Problems with Your FPGA

After the PCB design is complete, you can generate board-level SDF data for system-level simulation to ensure timing correctness. Full integration with SPECCTRAQuest™ provides easy access to powerful high-speed system design and verification features without spending time and effort in translations. You can verify signal integrity of all signals interfacing with the FPGA before you commit to manufacturing. This is very useful for the new high-speed FPGAs from Xilinx. SPECCTRAQuest also provides you with power plane modeling and EMC analysis features critical for high-speed designs.

All this can be done without any database translations or going out of the Cadence Board Design Environment. This ensures that your design intent is captured and carried from the beginning to the end of the design cycle. This integration with Cadence's PCB design solution makes design of high speed systems more reliable.

Conclusion

Concept HDL's powerful features for concurrent system and FPGA design, along with seamless integration with Cadence's PCB design solution, provides you with advanced capabilities to reliably design and verify large and complex system designs using FPGAs. It also allows for better and smoother communication between the system design and FPGA design. Using Concept HDL gives you the flexibility and power to effectively utilize the capacity of the latest Xilinx FPGAs without worrying about the CAD tools.

In the future, Cadence's Concept HDL will also provide features for concurrent design, generic data management, and other advanced features for system design. A tight integration with Cadence's new Integrated Native Complied Architecture for logic simulation will greatly speed up mixed language simulation.

For more details about the features of Concept HDL and other Cadence products, please visit the Cadence website at www.cadence.com or contact your local Cadence AE.

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