VeriBest's Vision of the Future

VeriBest, Inc., a Xilinx Alliance partner, remembers the early beginnings of EDA tools for Xilinx design, and provides a view of the future.

Remember the XC2000? I was a programmer in Huntsville, Alabama looking at designing an EDA environment for efficiently developing XC2000 and XC3000 designs. That was about ten years ago and the terms "Graphical User Interface" and "Design on NT" were unheard of in the design community. We've come a long way from the days of DOS command lines to the new vision of DesignView™ — VeriBest's hierarchical development environment that supports the top-down, middle-out, and bottom-up design methodologies necessary for the future of IP design reuse.

From Command Lines to Tri-Pane Design Desktops

Over the years, graphical interface design has become a key issue. You want to spend time on design, not memorizing command line sequences. Today, this environment is known as DesignView. Imagine a front-end design environment using multiple block views and multiple configurations allowing you to express "what if" structures in any combination of formats while simultaneously targeting multiple Xilinx families. Couple this ultimate expression of a design with seamless stimulus generation, LogiBLOX generation, integration with HDL simulators, synthesis tools, and Xilinx design tools. What you get is the power you need to have your designs meet schedule demands with the flexibility to explore your architectural alternatives; in essence, DesignView dramatically increases your productivity.

Providing much more than the flow managers of the past, DesignView allows you to *design the way you think* and view the design from the level most comfortable for you.

DesignView Work Surface

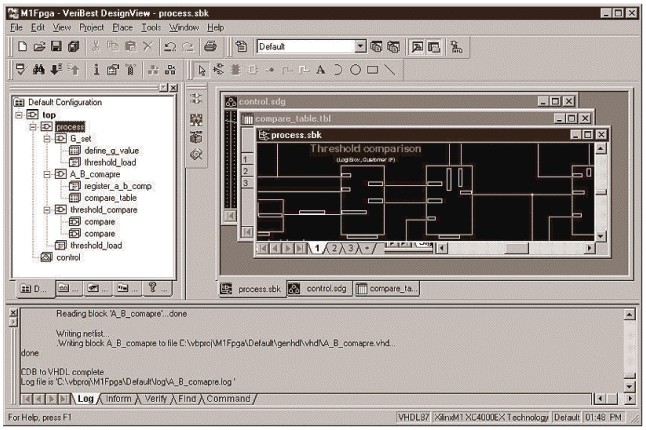

Figure 1

DesignView Work Surface

Let's look at DesignView's tri-pane work surface. The three work surface areas are:

- The Project Workspace area.
- The Design Editing area.
- The Output communication area.

The Project Workspace area contains five project tabs. These tabs allow you to access the:

1) Design hierarchy.
2) Design simulation environment (including associating and storing multiple stimuli for each hierarchical block).
3) Xilinx Place and Route files.
4) Project file manager.
5) Infoviewer (including links to the Web and Help files for VeriBest and Xilinx design tools).

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The Design Editing area is the workspace area for all the design editors. Your design may consist of schematics, graphical high-level designs (incorporating state diagrams and flowcharts), and HDL (hardware description language) designs in Verilog and VHDL. A workbook mode is available, allowing you to instantly access your design files from a tabbed workbook.

The Output Communications area provides reports on tool operations, such as design verification, project searches, and HDL compilations.

The implementation of this tri-pane window environment makes DesignView unique.

From Design Flows to Design Centric

Over the Xilinx 15 year history we have witnessed dramatic changes in design processes. The traditional top-down design flow now uses bottom-up flows that permit bottom-up verification. Middle-out flows permit synthesis and verification of single elements.

The primary failure of traditional design-flow-oriented EDA tools has been the limitations imposed on you. DesignView avoids this classic mistake by allowing all design process variants. In fact, DesignView is the only EDA tool that allows you to mix multiple design processes to complete a single design.

The DesignView design environment is “design centric” which gives you direct access to any block design file, allowing you to generate a block-specific stimulus and then send the block and its children to the HDL simulator, or to your synthesis tool, with a single menu click. DesignView’s unique design-centric environment gives you the flexibility you need to design from the top down, the bottom up, or the middle out.

Decide what block-specific operations you would like to perform using the Hierarchy Browser shortcut menu, as shown in Figure 2.

Hierarchy Browser Shortcut Menu

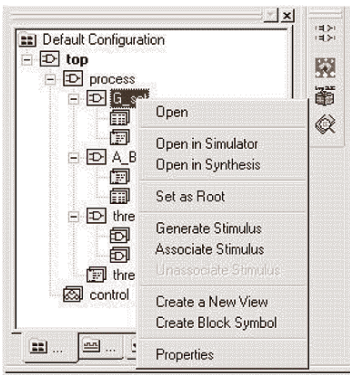

Figure 2

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You don’t need to worry about which HDL libraries to load into the simulators or which EDIF netlist switches to use — DesignView anticipates next tool use and automates tedious background configuration operations and file preparation for you.

Views and Configurations

Being able to view your design in a method most comfortable for you is unique with DesignView. You may create multiple views for each block in your design, by setting the “active” view from the hierarchy browser. Each block view has a corresponding design file in the Design Edit area. Display of the hierarchy is in a “default” configuration.

A configuration is the set of active block views, the selected root, the selected vendor technology, and the selected HDL language. You can create as many configurations as you want, and you can change parameters such as the vendor technology. Or, you can change the root and then simulate and route only a portion of your design, or even change the HDL language for some special simulation requirements. You can also switch between configurations and run “what-if” analysis without the hassle of recompiling or re-synthesizing; just set the configuration and you are off and running.

From X-BLOX to LogiBLOX Schematic Symbol Generation and Integration

As Xilinx moved from X-BLOX to LogiBLOX, providing even greater customization capabilities, VeriBest further enhanced LogiBLOX capabilities. The Xilinx LogiBLOX Module Generator is an integral part of DesignView, automatically generating symbols for each of your unique LogiBLOX macros. Your LogiBLOX macros appear in your Hierarchy Browser and appear to the simulator and synthesis tools as part of your HDL file list. The generated LogiBLOX symbols are identical to those displayed in the LogiBLOX selector helping you identify your unique LogiBLOX symbols on the schematic pages.

The word "dynamic" hardly describes the change that has occurred during these growing years for Xilinx, VeriBest, and the FPGA marketplace. Happy birthday Xilinx — from our view, the design future looks bright!

Design Reuse – From Graphical to HDL Based Design

The last 15 years have brought around more than just changes in design methodologies. HDL-based design and the emergence of VHDL caused us all to look at HDL generation as a key element. DesignView allows you to start your design graphically and then generate the version of HDL that you need. Taking a lesson from the programming community, reusable HDL design modules will be the future-DesignView is ready to meet that need now.

WaveBench™ – The Graphical Stimulus Editor

Part of the Design Editor offering is WaveBench. You invoke WaveBench directly from the design centric shortcut menu by selecting "Generate Stimulus" for the highlighted block. WaveBench provides you with the input signals and allows you to enter waveform data for each signal. Because you think of stimulus in terms of waveforms, we saw the need to have the ability to express stimulus in waveforms, with automatic HDL generation.

If you need more power, you can use Microsoft® Excel or Visual Basic, or Perl, to define your stimulus patterns and then read the information into WaveBench to display it, tweak it (when necessary), and then generate your new stimulus.

WaveBench Stimulus Generation Editor

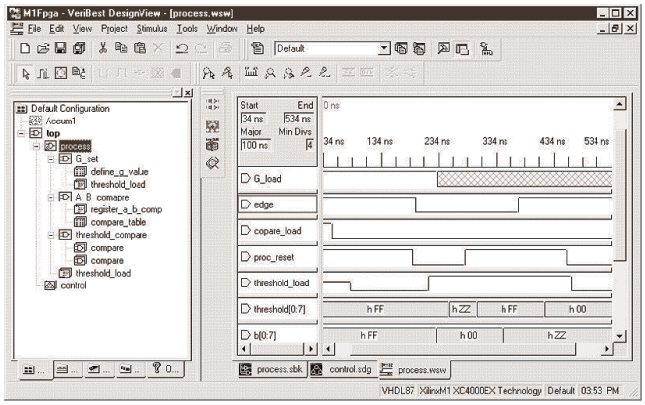

Figure 3

Emergence of HDL

With the emergence of design reuse, HDL design plays a more important role than ever before. VeriBest provides HDL simulation that's simply easy to use and ready to meet the language constructs needed for supporting the variety of synthesis processes used today. Launching simulation is seamless through the shortcut menu, allowing you to stay focused on your design.

Synthesis – Take Your Pick

DesignView supports both Synopsys FPGA Express 3.1™ and Synplicity Synplify® synthesis processing. DesignView automatically generates and manages the project files for your synthesis tool of choice. Your selected tool launches with the correct set of HDL files pre-loaded and ready for analysis.

Post-Synthesis HDL files are displayed to the Vendor Manager Tab of the Project Workspace letting you invoke the HDL simulator on the selected HDL file for a post-synthesis simulation session. Post-Synthesis vendor netlists are displayed in the Vendor Manager tab also. Once a vendor netlist is available, the Xilinx Designer icon is activated on the DesignView design kit toolbar. You are now ready to continue on to place and route.

Conclusion

The word "dynamic" hardly describes the change that has occurred during these growing years for Xilinx, VeriBest, and the FPGA marketplace. Happy birthday Xilinx — from our view, the design future looks bright!

For more information on DesignView, the core of the VeriBest FPGA Desktop product offering for Xilinx Design, visit http://www.veribest.com/sales/datasheets/3300/3300.htm. Σ