Inferring Virtex Block RAM with Leonardo Spectrum

Leonardo Spectrum, from Exemplar Logic Inc. helps you implement RAM in Virtex FPGAs.

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Two methods for implementing Virtex RAM are supported by Leonardo Spectrum:

- **Asynchronous RAM** is implemented from the memory elements contained within the lookup tables (LUTs). Leonardo Spectrum automatically detects asynchronous single-port, dual-port, and dual-bus RAM, from RTL behavioral models, and optimizes your implementation using LUT RAM.
- **Synchronous RAM** is implemented using Virtex Block RAM resources. All synchronous single-port, dual-port, and dual-bus RAM is now implemented using the Block RAM resource. Support for synchronous RAM is new, now available in Leonardo Spectrum 99.1, released in March, 1999.

Coding Examples

Synchronous, Single-port RAM Example

VHDL

```
architecture rtl of ram is

type mem_type is array (2**address_width downto 0)
 ofUNSIGNED(data_width – 1 downto 0) ;
signal mem : mem_type ;
 begin
 I0 : process (we,clk,address,mem,data_in)
 begin
 if (clk'event and clk = '1') then
 if (we = '1') then
 mem(conv_integer(address)) <= data_in ;
 end if ;
 end if;
 data_out <= mem(conv_integer(address)) ;
 end process ;
end RTL ;
```

VERILOG

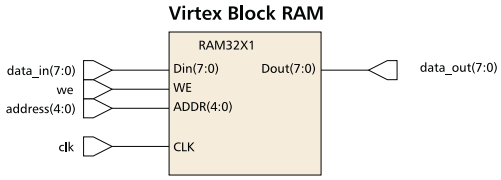
```
 module ram (data_in, address, we, data_out);
 parameter data_width=8, address_width=8,
 mem_elements=256;

 input [data_width-1:0] data_in;
 input [address_width-1:0] address;
 input we;
 output [data_width-1:0] data_out;

 reg [data_width-1:0] mem [mem_elements:0];

 always @(posedge clk) begin
 if (we) mem[address] = data_in;
 end
 assign data_out = mem[address];
endmodule
```

Table 1 – RAM Implementation Resource

	Single Port *Shared Data Port*	Dual Port	Single Port, *Separate Data Ports*	ROM
Synchronous	**Block RAM**	**Block RAM**	**Block RAM**	-
Asynchronous	**LUT RAM**	**LUT RAM**	**LUT RAM**	**LUT RAM**

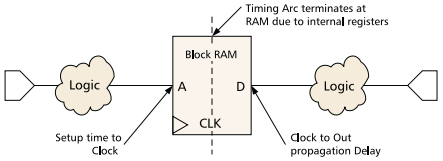
Resulting Circuit

There is no limit to the size of the RAM that can be inferred. Leonardo Spectrum will build up a RAM array out of available elements for a particular technology. In the above example two 32x4 RAMs are required.



Timing Analysis and Optimization

The Virtex Block RAM is a synchronous RAM; there are no asynchronous paths through the RAM. Leonardo Spectrum provides timing models for Block RAM which will generate input setup time and clock-to-out propagation delays similar to the way registers are modeled.



Device Resources

The current version of Leonardo Spectrum does not keep track of Block RAM resources and may implement more Block RAM than is available in the targeted device. If this happens you will need to disable block RAM inference on some blocks by setting the following variable:

```
> set extract_ram FALSE
```

Conclusion

Block RAM can dramatically improve the utilization of a Virtex device. By having dedicated resources, memory can be implemented in a Virtex device without sacrificing lookup tables that are used for random logic. Leonardo Spectrum's inference capability makes it easy to design in Block and LUT RAMs.

For more information about Exemplar Logic, Leonardo Spectrum and Block RAM inference, visit our website at www.exemplar.com or contact Exemplar at 510-789-3333. Σ