HOW Times HAVE Changed

Reminiscing about the "good old days."

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In 1986, not long after slide rules went out of style, one of my first assignments as an engineer was to design an ASIC for an industrial controller. The design was entered into schematics using an 8086-based PC. Simulation was accomplished using a hardware accelerator that could run just over 100 test vectors a second. We only had one hardware accelerator, with two ASIC designs going on at the time. Because my project had lower priority, I had to work nights to guarantee access to the accelerator. Otherwise, I had to use the PC-based simulator, capable of about two to three vectors per second. If I had not worked nights, I might still be simulating that design.

My first ASIC design used approximately 2,000 gates, ran at 10 MHz, and had 20 TTL level I/Os. NRE for the chip was around $15,000 and the chip price was about $15.00. The design took six to eight hours to place and route on a PDP-11 mainframe computer. At that time FPGAs had been available for about a year and using two XC2018s would have offered a $130 solution to the problem. However, FPGAs were too new, and too expensive to be a viable contender for this design. Besides, who was this company Xilinx, and would they be around in 10 years, at the end of this product's life cycle?

About five years later, I designed a video acceleration card and used a Xilinx XC3090 to perform a pixel mixing algorithm. By this time FPGAs were considered a proven commodity, and Xilinx was a "household word" in the engineering community. The design used approximately 7000 gates, ran at 25 MHz, and had 95 TTL level I/Os. The chip cost was about $150. At that time, the Xilinx XACT software, running on a 33 megahertz 80386, could place the design in four to six hours. My compile times had dropped significantly, and I could do it on my desktop, instead of on a mainframe, and I was able to work daylight hours. This was real progress.

Now it's 1999 and I've been a Xilinx employee for three years. On a recent customer visit, an engineer gave me a design implemented in VHDL. As we talked, I targeted the design at the Virtex family, using the Foundation Express software. The design had nearly 150 I/Os, with 96 of them being GTL-compatible. I was able to fit the design into a 50,000 gate Virtex device, as we talked, and the design ran at over 100 megahertz. Overall, I placed and routed the design three times on my notebook computer, during our 2 hour meeting.

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It's amazing how the world has changed for Xilinx over the past 15 years. The ASIC vendor that I had used in my first design has disappeared, taking the ASIC with it. On the other hand, the Xilinx XC2018 was in full production until about two months ago. I've gone from using a room full of computers to place and route a 2000 gate ASIC to using a 10 pound notebook computer to place and route a 50,000 gate Xilinx FPGA. Design speeds have jumped from a few megahertz to over 100 MHz. Compile times have been drastically reduced from a work day to a coffee break. In 1985, a 64-bit shift register would consume an entire XC2064, today it would fit in a single Virtex CLB.

Of course, technology keeps marching on. We already have two-million gate devices on the drawing board, and in our laboratories, we have devices running at gigahertz speeds. Our development software is continually being improved, both with our in-house development and with tools and technologies from our EDA partners. And, we continue to create new enabling technologies such as our Silicon Xpresso software that allows you to modify and test your FPGA designs, at your customers' locations, anywhere in the world, over the Internet.

There's no end in sight to the possibilities offered by programmable logic. ✖