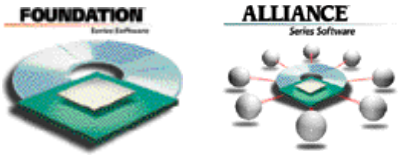

New 2.1i Software – Shortens Design Cycles, Improves Productivity

The latest releases of the Xilinx Alliance Series and Foundation Series software are now available.

by Arne Barras,Product Marketing Manager, Xilinx, arne.barras@xilinx.com

There are many new productivity-enhancing features in the new 2.1i software release from Xilinx. Faster runtimes, quicker constraint entry, better timing reports, and the most recent update of FPGA Express all combine to shorten the amount of time it takes to complete a Xilinx design. Almost every tool, from mainstream applications like the Design Manager/Flow Engine to advanced ones like the FPGA Editor, has been enhanced with new features that make it easier than ever to get great results quickly when using Xilinx programmable logic.

2.1i Overview

Xilinx Development systems are packaged in two product families, each configured to provide the tools necessary to support any customer's design flow needs. Both families of design solutions include the world-class Xilinx implementation tools, the industry's leading solution in advanced programmable logic design methodologies.

The Xilinx Alliance Series™ solutions emphasize seamless integration into Alliance EDA partner design flows and methodologies. This release of the Alliance Series software features support for LMG Smartmodels, enabling board-level simulation, and chip-level I/O timing models written in the Stamp format, enabling board-level static timing analysis. Alliance Series solutions also drove the requirements for the addition of other ASIC-like design capabilities, such as minimum delay reporting, and temperature and voltage prorating.

The Xilinx Foundation Series™ solutions are ready-to-use programmable logic design packages. Incorporating all facets of design into a complete, front-to-back design environment. The Foundation Series emphasizes ease of use in simplifying the programmable logic design flow.

While simplifying the design process, Xilinx has also managed to incorporate some of the industry's best schematic and HDL design and synthesis technologies in a package with a price tag that is hard to beat. The v2.1i Foundation Series solutions feature FPGA Express™ v3.2, synthesis technology that delivers the robust language compilation capabilities designers have become accustomed to receiving from Synopsys, with new Xilinx-specific optimization capabilities. A more detailed review of the new features in the 2.1i products is provided below.

New Features in the v2.1i Implementation Tools

This section discusses the new features that are common to both the Alliance Series and Foundation Series products.

Runtime Improvement

Development efforts toward reducing runtimes were focused on the Virtex family, and this has paid off with a 50% reduction in runtimes for the larger Virtex devices. This runtime improvement is concentrated mostly in the placement step, which can be anywhere from four to ten times faster than the time required for placement in version 1.5i. This improvement in runtime comes with no performance penalty; clock

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rates should be as fast or faster than those obtained from the 1.5i software.

2.1i Hierarchical Timing Report Browser

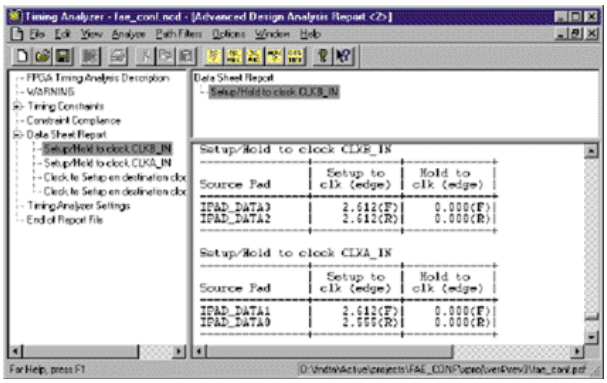

Figure 1

Timing Reporting and Analysis

One of the most visible enhancements in the 2.1i software release is in the area of timing reporting. A new "datasheet style" timing report saves you time by simply and clearly displaying all I/O timing of the chip as well as clock frequency. The I/O timing includes input setup and hold, as well as output clock-to-pad analysis, and the clock frequency is reported on a per clock basis.

For more complex designs such as those that include multiple clocks, separate tables are provided that report the phase relationships between each clock domain. By default, this report will list the delays for any I/O or clocks with timing constraints on them. For designs without timing constraints the report can be generated by selecting the "Advanced Analysis" option in the Timing Analyzer.

Another great new timesaving feature is the hierarchical timing report browser (Figure 1) available from the within the Timing Analyzer. By generating and viewing timing reports from this tool, even the most detailed and complex timing reports are easily navigated.

Virtex Floorplanner

The Xilinx Floorplanner (Figure 2), first introduced in our 1.5i release, has been enhanced to support the Virtex device family. It offers a simple graphical view of the physical design, simplifying the process of floorplanning a design, and thus leveraging user knowledge to simplify the algorithmic intensive process of laying out a design. Floorplanning has proven to be most useful for larger, highly structured designs. The Floorplanner is accessible both from the Design Manager and from the command line.

2.1i Floorplanner

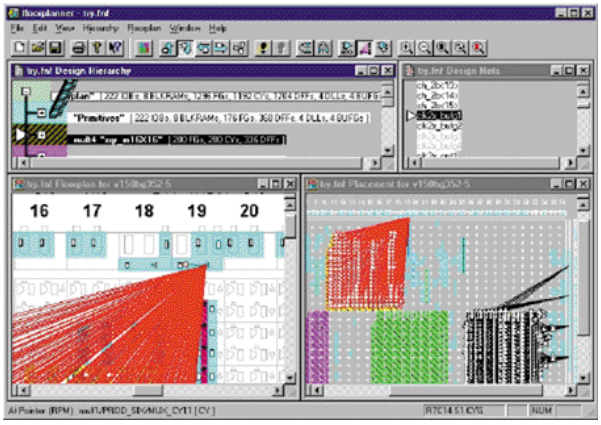

Figure 2

Support for Board-level Static Timing Analysis

The value of static timing analysis, as a complement to simulation to reduce timing verification, has long been recognized within the FPGA design community. This methodology is now being extended to support board-level design as well. Xilinx can now generate a Stamp timing model of the device I/O, for use with BLAST™ from Viewlogic, or Tau™ from Mentor Graphics - two of the more popular and powerful board-level static timing tools available today.

The Stamp timing model is generated using the **-stamp** command line option of TRCE, the static timing analysis command, or by adding the **-stamp** option to the Design Manager through its Customize capability.

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Design Manager

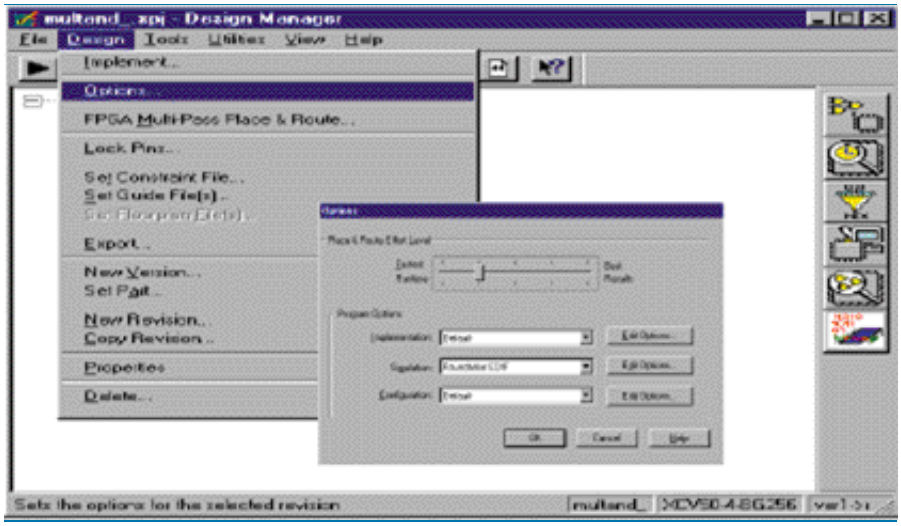

Figure 3

Design Flow Automation Improvements

Compiling a design through the Xilinx Design Manager has become more streamlined through several new enhancements:

- Run-time options have been made more visible and easy to find by moving them up a level from the Implement dialog, to an "Options" command directly accessible from the "Design" menu.
- Fewer revisions are created in the 2.1i release because the Design Manager will continue to implement a design within the current revi sion unless the input netlist has changed.
- The new, "Smart" Flow Engine automatically detects which options have been changed or if constraint tools like the Constraints Editor or Floorplanner have been used, and implements the modifications by starting at the appropriate step in the flow. This simplifies the design flow by not requiring you to manually choose which steps are to be run, and shortens runtimes by removing the requirement to start the implementation process from the beginning as a result of any design constraint modification.

Another significant enhancement in the Design Manager (Figure 3) is the capturing of options and control files such as the constraints file, guide file, and floorplan into the revision itself. Combined with the "seed file" capability that is already in the 1.5i release, any revision can now be considered a full snapshot of the files and options to produce that revision. At any point in time, you can review not only the results of a revision, but the options and files used to produce it.

Real-time Debugging

A new real-time design debug capability has been added in the 2.1i release. This capability allows you to identify any internal signal that you wish to see externally, and it will be automatically routed to an unused I/O pin. Called "PROBE", it is accessed through an easy two-step process of selecting the desired internal signal and choosing one or more available I/O pins to display it on.

There is no limit to the number of internal signals that can be probed, and they can be selected and brought out without having to re-implement the design. PROBE is available in the new FPGA_Editor. Replacing the older EPIC tool, the new FPGA_Editor is a fully MFC-compliant rewrite which brings many advantages such as being able to open multiple windows and view more than one area of the FPGA at one time.

Constraints Editor

High speed designs often require a complete set of timing constraints, and the 2.1i Constraints

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Constraints Editor

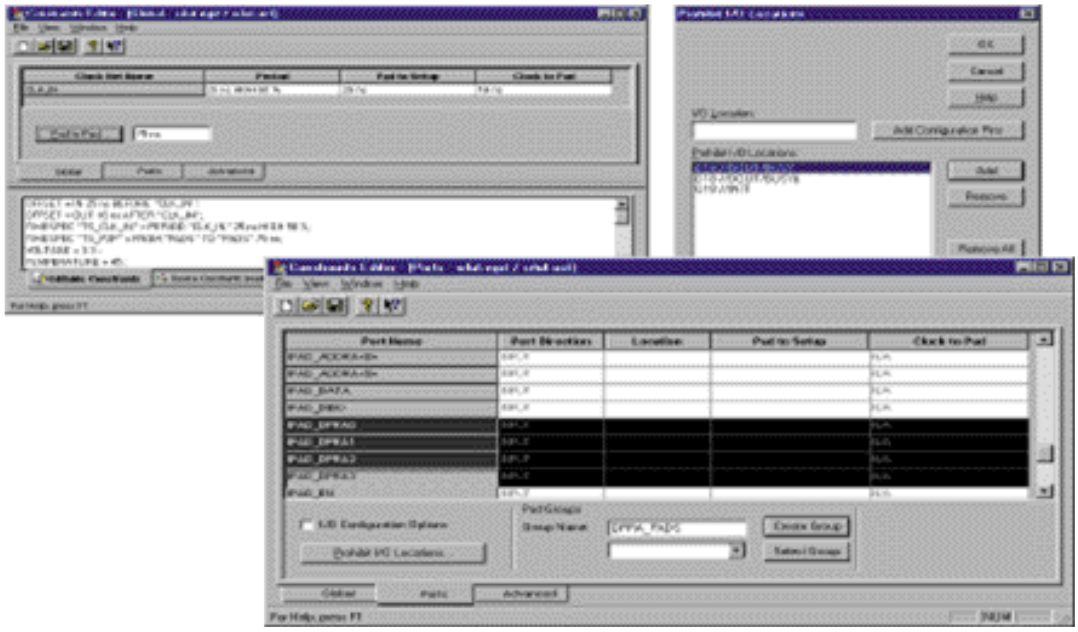

Figure 4

Editor (Figure 4) has been enhanced to shorten the amount of time it takes to apply them. These enhancements include direct cell entry similar to that found in spreadsheet programs, the ability to select multiple cells at once, and the ability to easily group pads together and apply a single constraint. Together these all help reduce the effort needed to enter timing constraints.

Easing the overall design constraining process is the addition of a command to prohibit the dual-purpose configuration pins during layout, and the capability to specify the Virtex I/O attributes such as Pullup, Pulldown, Keep, and the various voltage standards and drive capabilities. DLL support for Virtex has also been improved, now automatically adjusting and applying the constraint to the DLL outputs, and allowing just the input clock to be specified.

Minimum Delays and Prorating

Minimum and prorated delays, which were initially introduced for the XC4000XL family in the1.5i release, have been extended to support the XC4000XLA™ and SpartanXL families in the 2.1i release. The 2.1i release has also been designed to support minimum and prorated delays for Virtex FPGA as soon as the values are provided in an upcoming speedfile, which is on support.xilinx.com.

New XFLOW Scripting Tool

For those who prefer to run the tools using a command line, through batch files, or want to encapsulate the Xilinx implementation tools into their own shell programs, a new tool named XFLOW has been added. It allows you to pick from a set of predefined flows and option files and run the entire implementation process as a single command. In addition, you can modify the flows and options to create your own preferred set.

Foundation Series Software Improvements

The Foundation Series software builds on the strength of the features described above by incorporating the latest version of the Xilinx implementation tools. This update has integrated user access to each of the advanced analysis tools offered by Xilinx in the Foundation tools, and expands the design implementation flow options available to Foundation users. This feature expansion also adds the options of guided

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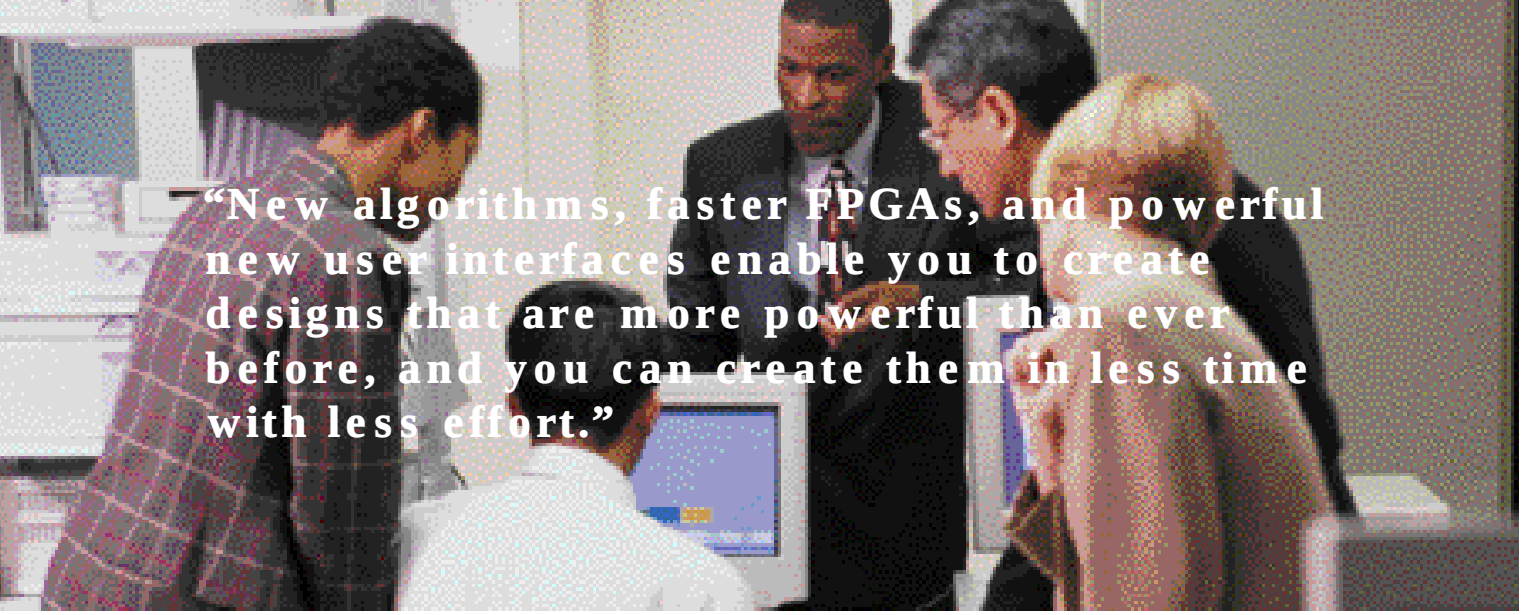

implementation flows as well as utilization of floorplan data. In addition, the Foundation Series software further improves productivity and shortens the design cycle time by adding several other productivity enhancing features.

Foundation Design Entry Tools

One of the productivity enhancements that schematic users will notice is the addition of several Design Rule Check (DRC) options in the Foundation Series schematic editor. This release also so you can select the DRCs that are performed, allowing you to avoid unnecessary warnings and messages.

The second item that you will notice is the integration of the Xilinx CORE Generator™ tool. You now have access to Xilinx cores without leaving the Foundation Series environment. Simulation models, HDL instantiation templates, and schematic symbols are all automatically added to your environment.

Foundation Series Synthesis Engine

The Foundation Series synthesis flow has become more efficient with the integration of the latest FPGA Express synthesis technology. The 3.2 version of the FPGA Express synthesis engine dramatically improves multiplier implementations, delivering smaller and faster multipliers. The FPGA Express synthesis engine also offers options for buffering internal nets, so you can automatically take advantage of unused global routing resources for internally generated high fanout nets.

The implementation timing constraints, forward annotated by the synthesis engine, have also been improved to reduce the overall design cycle. The FPGA Express engine writes timing constraints which have been optimized for the Xilinx implementation tools, requiring fewer system resources and improved runtimes.

Summary

Version 2.1i of the Xilinx Alliance Series and Foundation Series software adds many new productivity enhancements. While the previous release of these solutions, (v1.5i) was highly acclaimed as the fastest and easiest to use in the industry, the 2.1i release is even faster and easier to use. New algorithms, faster FPGAs, and powerful new user interfaces enable you to create designs that are more powerful than ever before, and you can create them in less time with less effort.Σ

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