# A New Family of In-System Programmable *FLASH* Serial/Parallel PROMs

*Programming, storing, updating, and delivering bit streams for programmable logic has just become a lot easier.*

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Xilinx recently introduced a whole new family of JTAG in-system programmable, serial/parallel PROMs. The new XC1800 family uses the IEEE 1149.1 Boundary-Scan interface (commonly know as JTAG) and enables you to easily and cost-effectively configure an FPGA. The XC1800 family can easily interface to any Xilinx FPGA, including the Virtex and Spartan families, using a simple interface requiring only one user data pin. For the ultimate in download speed, these PROMs accommodate the 8-bit wide Select Map and Express modes that enable bit stream rates as fast as 500 Mbits per second.

| Device | Configuration Bits |
|--------|--------------------|
| 1804 | 4,194,304 |
| 1802 | 2,097,152 |
| 1801 | 1,048,576 |
| 18512 | 524,288 |
| 18256 | 262,144 |
| 18128 | 131,072 |

*Table 1 - Product listing*

## Flexible Bit Stream Reconfiguration

The XC1800 series makes it very easy to do power-on downloading and field updating of bit stream files. The power-on loading of the FPGA is enabled automatically, and if the configuration of the FPGA needs to be changed during operation (to remotely download hardware enhancements, debug configurations, or fix bugs, for example), the XC1800 series can be reprogrammed remotely using the JTAG port and then the bit stream is downloaded to the FPGA, without first powering down the FPGA. The FPGA can also be reconfigured directly from the JTAG port, without affecting the bit stream stored in the PROM.

## Features:

- Densities ranging from 128 Kbits to 4 Mbits.

- Endurance of 10,000 program/erase cycles.

- Fast programming and configuration speeds.

- Dual configuration modes.

    - Serial Slow/Fast configuration (6 to 15 mHz).

    - Parallel

- PROM controlled initiation of configuration without powering down FPGA.

- IEEE Std 1149.1 Boundary-Scan support.

- JTAG command initiation of standard FPGA configuration.

- Cascadable for storing longer or multiple bitstreams.

- I/O pins accept 5 V, 3.3 V, and 2.5 V.

- 3.3 V or 2.5 V output capability.

- Available in PC20, SO20, PC44, and VQ44 packages. Σ

For more information see:
http://www.xilinx.com/products/configsolu.htm

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