Try HDL Simulation for Free

Xilinx and Model Technology have partnered to give you a risk-free introduction to HDL simulation.

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You probably already know why using VHDL or Verilog is such a good idea, and you may already be using a high-level description language (HDL) to represent your design. You may be coupling HDL with synthesis, and simulating your design with a gate-level simulator to confirm its behavior after synthesis. However, when it comes to verifying your design, are you still relying on the time consuming method of testing programmed devices in a prototype? If so, here is a better way.

As your designs get bigger and your design cycles get shorter, physical verification becomes too time consuming and costly. However, with the ModelSim Xilinx Edition Starter (XE Starter) and ModelSim Xilinx Edition (XE) software, you can try VHDL or Verilog simulation and begin to leverage the full power of an HDL-based design flow.

Why Use HDL Simulation?

Even if you are not trying to squeeze three whole circuit boards onto a single Virtex device, your next design will probably be bigger than your current design. The benefit of a full HDL design flow that includes HDL simulation is simple: you will get your designs fully debugged and working in the system, faster.

HDL simulation allows you to debug your design at the source code level, pinpointing design problems directly to the line of code responsible for the failure. For example, you can stop the simulation whenever a variable changes, or step through a piece of code line by line, or trace a signal's flow through a design.

You can write tests in VHDL or Verilog which not only apply stimulus to your design, but which can check for the correct response. The same "self-checking testbenches" can be used before synthesis, after synthesis, and after place-and-route. Not only is it easier to let the testbench inspect the design for failures, but it will improve quality as well.

HDL simulation also allows you to explore alternatives and determine design tradeoffs quickly. You can create powerful designs with thousands of logic gates in just a few small modules of high level VHDL or Verilog code. And you can make major changes to the design quickly, and simulate those changes without running any synthesis or implementation tools.

The Right HDL Simulator for YOU

ModelSim is the most popular HDL simulator on the market, with over 40,000 licenses sold to date. This success is grounded in ModelSim's performance, value, ease of use, and broad industry support. Now, with the introduction of ModelSim XE Starter and ModelSim XE, Model Technology and Xilinx are working together to ensure that you have the tools necessary to meet all your HDL design and verification needs. With Model Technology and Xilinx as your partners in

	ModelSim XE Starter	ModelSim XE	ModelSim PE	ModelSim SE/EE
	Available from Xilinx	Available from Xilinx	Available from Model Technology	Available from Model Technology
100% compilant VHDL or Verilog simulation	X	X	X	X
Complete HDL debugging environment	X	X	X	X
Windows 95,98,NT Support	X	X	X	X
Unix Support				X
Appropriate for Device Densities in the range of:	Less than 500 lines of HDL code	Xilinx 9500, Spartan, low-density 4KX and Virtex FPGAs up to approximately 60k gates*	Most CPLD/FPGA designs	All designs, including extremely large FPGA and ASIC designs
Typical simulation times for medium sized design and test set	10 minutes	10 minutes*	2 minutes	30 seconds
Support for mixed VHDL/Verilog designs			X	X
Language-neutral licensing				X

*Simulation performance for ModelSim XE diminishes by a factor of 2x for designs with more than 4000 lines of RTL HDL code, and by an additional 10x for designs with more than 30,000 lines of RTL HDL code. See www.model.com for more ModelSim PE/EE/SE differences.

Table 1 - ModelSim Versions

design, you are certain to get to market quicker, helping make you and your project successful.

Features:

- **Proven technology**–the most widely used HDL simulator in the world.
- **Easy-to-use**–fast, comprehensive debugging with a full-featured graphical interface.
- **Powerful**–has the performance and features for even the most demanding designs.
- **Flexible**–handles VHDL, Verilog, or even mixed-language designs.
- **Scalable**–configured to meet a variety of performance, capacity, and budget demands.

ModelSim Xilinx Edition Starter (XE Starter)

The ModelSim XE Starter version is a risk free solution for learning the benefits of VHDL or Verilog simulation. This product enables new HDL designers to experiment with the simulation of small HDL designs. ModelSim XE Starter is provided free of charge to all registered Xilinx customers who have current maintenance contracts.

ModelSim Xilinx Edition (XE)

ModelSim XE provides a powerful step into the world of HDL simulation with capacity and performance designed for verifying Xilinx XC9500 CPLD series and Spartan FPGA series of programmable logic devices, as well as for the lower-density versions of the XC4000 and Virtex FPGAs. ModelSim XE supports behavioral, RTL, and gate-level simulation of Xilinx cell libraries and is available in both VHDL and Verilog versions.

Conclusion

The ModelSim family of products also includes the ModelSim Special Edition (SE) and Elite Edition (EE) for cutting-edge ASIC and high-end FPGA development on both PCs and Unix workstations. Also available is ModelSim Personal Edition (PE), the price/performance leader for PC-based FPGA designs. ModelSim SE, EE, and PE are available for purchase through MTI and its distributors (see www.model.com for more details).

The industry's most friendly upgrade program guarantees that you can begin using ModelSim XE today, and leverage your investment tomorrow for an upgrade to the more flexible SE, EE, or PE products as your verification needs change.

For more information on ModelSim XE Starter and ModelSim XE see:
www.xilinx.com/products/software/mxe.htm