The Spartan-II Design Flow
Simple, Powerful, Efficient

A design flow that offers distinct advantages when compared to an ASIC design methodology

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With the rapid adoption of deep-submicron process technology in the design of FPGAs, Xilinx is now able to provide you with a cost-effective alternative to using an ASIC. But the cost of silicon is only one reason why the use of Spartan devices in high-volume applications is skyrocketing.

Spartan devices are designed using our robust suite of design tools. These tools have become rich in features as a result of the inclusion of a series of patented innovations. This article describes some of the key technologies that are included in the Xilinx development systems, including HDL optimized flows, timing driven layout, core (intellectual property) design and integration, and a comprehensive suite of verification tools.

Xilinx design methodology also offers some distinct advantages when compared to an ASIC design flow. These improvements in the art of logic design deliver benefits that reduce the cost of design development and accelerate time to market.

A Robust Suite of Design Tools

The development systems that Xilinx delivers today incorporate the collective innovations of over 15 years of programmable logic design expertise. These improvements to the programmable logic design process have resulted in the creation of a comprehensive, high quality suite of design tools. Xilinx development systems are packaged to deliver the best value for your dollar, enabling you to invest in just what you need to get the job done.

All Xilinx development systems include a comprehensive set of key technologies that enable the efficient design of powerful, high performance products. Other tools useful in the design of programmable logic are delivered as options or as part of the Foundation Series "packaged" solutions, including HDL design, simulation, synthesis, and optimization.

One of the benefits of programmable logic is the ability to program (and reprogram) the device at your desktop. In order to do so, you need a set of tools that take your design from concept to silicon. Processing your design includes design capture (including HDL synthesis

and/or schematic entry), implementation, and verification.

Capturing your Design

The first step in the creation of any logic design is to capture the intended functionality in electronic format. While Xilinx has a rich history in the support of schematic capture programs, over the last six years Xilinx has been working with leading vendors in support of HDL design flows (synthesis and optimization). This investment is paying dividends to designers using Xilinx devices in terms of technology specific optimizations that enable the creation of high performance designs from VHDL or Verilog.

The Xilinx Foundation Series™ software includes synthesis capabilities from industry leader Synopsys® (FPGA Express™). To ensure the highest quality of results through the synthesis process, Xilinx works cooperatively with all synthesis partners to develop proprietary optimization technology for Xilinx devices. This technology takes advantage of the extensive knowledge that the Xilinx R&D staff have of its silicon and implementation tools. These improvements are developed in a manner which allows them to be shared with third party synthesis vendors to ensure high quality results, through HDL design flows, regardless of your chosen synthesis provider.

Xilinx also delivers the industry's best design reuse methodology, enabling the seamless integration of intellectual property from either third parties (Alliance cores) or Xilinx (LogiCores). The Xilinx CORE Generator™ enables the customization of the core's parameters at your desktop, creating the exact functionality that your design requires. The use of SmartIP™ technology in the creation of cores ensures predictable, high-performance, scalable functions. One of the most popular cores is the Xilinx PCI LogiCore, currently offered as both 32-bit/ 33-MHz and 64-bit/66-MHz interfaces.

Implementation

Xilinx patented the timing-driven place and route of FPGAs in the early 90s. This technology allows you to specify timing requirements when creating your design, and automatically optimize your design with these requirements in mind. Advanced integration, between the synthesis tools and the Xilinx implementation tools, enable the passing of timing requirements from synthesis to place and route, and circuit delay information from place and route back to the synthesis algorithms.

This closed loop methodology not only saves time, by making sure that the place and route tools are working to create a design that meets all of your system needs, it also provides immediate feedback when timing requirements are unrealistic, given the current design description. In fact, the flexible verification methodology that Xilinx provides ensures that you are given feedback on the feasibility and quality of your design throughout the design flow. This Checkpoint Verification™ process ensures that you are spending your time most efficiently. The process

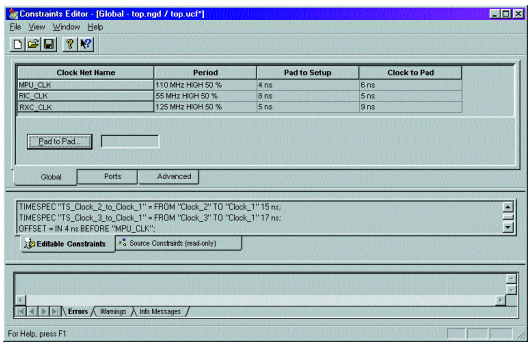

Figure 1: Constraints Editor

continues only with design iterations that will converge on your overall system requirements, and identifies trouble spots in designs that will not.

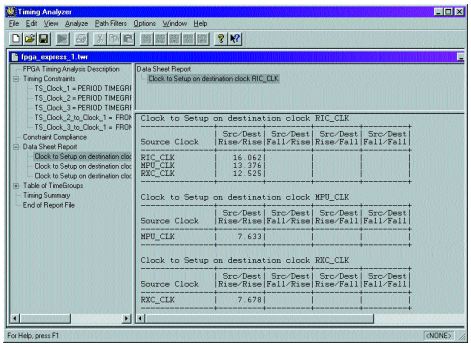

Figure 2: Timing Analyzer

Xilinx has also made great strides in simplifying the process of timing driven design. The Xilinx “Constraints Editor” (Figure 1) guides you in your selection of signals and nodes to which you will apply timing constraints within your design. The Signal and Node lists are based on the same names you provided during the creation of the schematic or HDL source.

This easy-to-use GUI provides an intuitive interface for using industry’s most comprehensive timing specification language—TimeSpecs™. Once these timing requirements are specified and the design is implemented, the Xilinx Timing Analyzer (Figure 2) is used to analyze the performance of a design. This intuitive interface streamlines the process of evaluating your designs timing by enabling a hierarchical analysis of all of the design’s timing paths through the use of (+) expand and (-) collapse functionality.

The key to many design flows is the ability to rapidly iterate between design capture, implementation, and simulation (or in-system test). Iterative design is one key advantage of using programmable logic in your system, and to best take advantage of this, fast compilation times are important. To this end, Xilinx has dramatically reduced the place and route compilation times for its Spartan-II and Virtex families. Where traditional FPGA design flows implement designs at approximately 10K gates per minute, Xilinx v2.1i tools compile designs at a rate of approximately 100K gates per minute. For Spartan-II devices this translates into place and route times as fast as 1 minute, with average run times less than 10 minutes.

Verification

The increased density and performance of programmable logic is resulting in its frequent use as the central component in equipment design. As such, the emphasis on verification of programmable logic designs is becoming paramount to a program’s success. Xilinx Check Point Verification methodology provides all of the hooks necessary to verify the operation of your design within the FPGA and within the target system. Elements of the Xilinx checkpoint verification model include:

- Support for functional, gate, and timing simulation.
- LMG SmartModel™ support for the Xilinx FPGA.
- Chip-level static timing analysis.
- STAMP™ model generation for board-level static timing analysis.
- In-System debug with Probe™.

Through this comprehensive suite of verification tools and data files, Xilinx provides you with the ability to employ the verification methodology of your choice. Our close relationships with

our Alliance EDA partners ensure success in the use of partner tools, while Xilinx also offers the Foundation Series solutions as a complete, ready to use package of EDA and place and route tools, automating both design compilation and verification.

Improving the Art of Logic Design

The Xilinx design methodology leverages the technological advantages of programmable logic, including the fact that all devices shipped by Xilinx are 100% functionally verified at the factory. This fact alone translates into weeks of savings in design time, as the processes of scan insertion and the re-verification of a design after scan insertion is not required.

Another key benefit in the Xilinx design flow is that the device is ”fabricated“ (programmed) by you, at your desktop, or in your manufacturing organization. Your retention of control of this process means that there is no Non-Recurring Engineering (NRE) cost associated with the creation of the device. This can dramatically reduce the emphasis frequently placed on running comprehensive (and time consuming) timing simulations after layout, and before device ”fabricated“.

For programmable logic, a relatively comprehensive verification regimen can consist of functional verification and static timing analysis if good synchronous design practices are followed. The streamlined Xilinx design flow reduces the necessity of timing simulation, which is frequently a time consuming process. If your environment calls for the verification of your chip design within the board (or system), Xilinx also generates the necessary timing information for use with board-level static timing analysis or simulation tools.

The ability to program the Xilinx device at your desktop also means that you can quickly iterate your design in a ”burn and learn“ fashion, reducing the pressure to get it right the first time. Problems discovered during in-system verification can actually be remedied in the chosen logic device. This is particularly useful when industry specifications or marketing requirements haven’t stabilized prior to the beginning of your project.

The combination of these factors means that the design methodology that you follow is streamlined when compared to the process required to design with an ASIC. The time saved in the design flow and system verification is frequently dramatic.

Conclusion

The advantages of creating your design with programmable logic include more efficient use of your time, faster time to market, and no NRE costs. Our experience has found these benefits frequently result in improved market success of our customers’ products. In addition to these benefits, the development systems required to design a Spartan device into your product are configured and priced to comfortably fit within any budget. Visit The Silicon Expresso Cafe (the Xilinx on-line store) or contact your local Xilinx sales representative to learn more.