Inverse Multiplexing for ATM (IMA)

A Programmable ASSP Solution for transmitting high-bandwidth data over multiple T1 or E1 lines.

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The Spartan-II Family, combined with an extensive soft intellectual property (IP) portfolio is the first programmable logic solution to effectively penetrate the ASSP marketplace. The ATM IMA-8 core from Applied Telecom, ported to the Spartan XC2S150 device, is a good example, highlighting the concept of a programmable ASSP.

Applied Telecom is the newest member of the Xilinx AllianceCORE program and brings a wealth of expertise in ATM, SONET, telecommunications, and networking applications. The IMA-8 core, developed, sold, and supported by Applied Telecom, targets network access systems such as adapters, multiplexers, and switches. Several leading manufacturers, including Alcatel, Ericsson, Nokia, and Nortel, are already using Applied Telecom's Xilinx-based IMA technology in production systems.

What is IMA?

IMA stands for "Inverse Multiplexing for Asynchronous Transfer Mode" (ATM) and it allows the transmission of a high-bandwidth stream of ATM cells over multiple T1 (1.544 Mbps) or E1 (2.048 Mbps) facilities (or circuits). IMA is applicable to both public and private networks and allows end users to enjoy the many benefits of ATM, such as Quality of Service (QoS) provisioning, scalability, and the ability to easily mix data, voice, and video. IMA circumvents the high cost and unavailability of broadband transmission facilities such as T3, E3, and SONET/SDH by using only as many lower cost, lower bandwidth facilities as necessary. With the advent of Digital Subscriber Line (DSL) technology, the case for IMA is even greater.

IMA Applications

IMA is applicable to many different types of ATM Wide Area Network (WAN) access equipment including ATM switches and routers with WAN ports, ATM access concentrators and multiplexers, and communications servers with WAN NICs. Typically, IMA is used as the WAN interface for general purpose access multiplexers, traffic aggregators, and access switches. Another common application is in Digital Subscriber Line Access Multiplexers (DSLAMs) where IMA can be used either to interconnect the DSLAM with a Remote Access Multiplexer (RAM) or as the high speed network-side interface. Emerging applications are extending the IMA protocol beyond T1 or E1 to include other facilities using DSL circuits.

IMA Operation

Figure 1 illustrates the basic IMA mechanism for sending a single ATM cell stream over a number of lower speed transmission facilities or links.

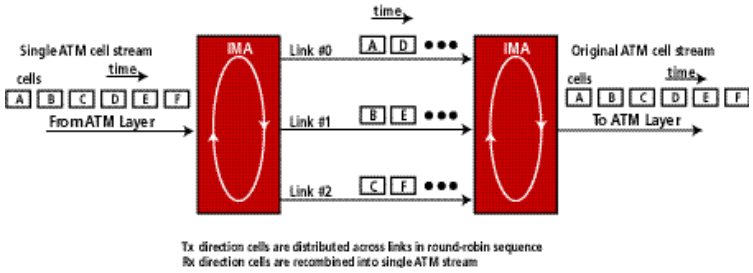

Figure 1 - Simplified IMA process.

Layers	Sub-layer	Functions
ATM Layer		
Physical (PHY) Layer	IMA Specific Transmission Convergence Sublayer	ATM cell stream splitting and reconstruction
		Differential delay accommodation
		IMA Control Protocol (ICP) cell insertion / removal
		Cell rate decoupling
		IMA frame synchronization
		Cell stuffing,asynchronous facility compensation
	Interface Specific Transmission Convergence (TC) Sublayer	Discard cells with HEC errors
		Header error correction
		HEC generation / verification
		Cell scrambling / descrambling
		Cell delineation
		Scrambling / descrambling
	Physical Media Dependent (PMD) Sublayer	Transmission frame generation / recovery
		Bit timing,line coding
		Physical medium

Table 1 - IMA sublayer reference model.

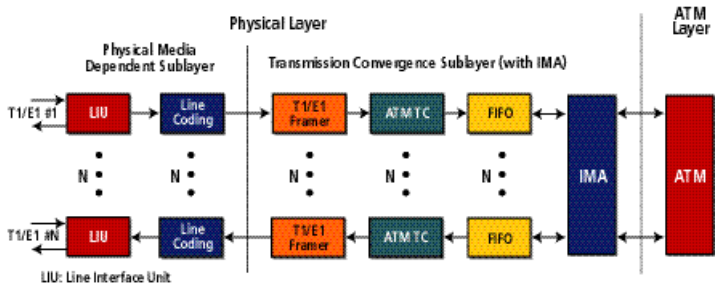

Figure 2 - Typical PHY implementation.

When splitting an ATM virtual circuit among multiple T1 or E1 links, the IMA subsystem must insert the IMA-specific cells into the transmitted ATM cell streams. In the receive direction, a cell-based IMA framing process is used to locate and remove the IMA-specific cells so that only the ATM cells are passed to the ATM Layer.

A variable number of physical links and ATM bandwidth rates can be supported and mechanisms are specified for accommodating differential delay variations present in the transmission links and for handling link failures and changes to the available transmission bandwidth.

Layer Reference Model

In terms of the protocol layer reference model, the IMA sublayer is considered to be an extension of the Physical Layer (PHY), sitting below the ATM Layer (ATM) and, as much as possible, transparent to the ATM Layer device. Table 1 illustrates the functions performed by the IMA sublayer.

From an ATM layer perspective, the behaviors exhibited by IMA groups are different than those of real PHY facilities. Two examples include the effects of IMA group start-up and variations in bandwidth caused by the activation/deactivation and addition/deletion of links.

In addition to the PHY layer, IMA also affects the management layer. The management layer handles alarm detection and processing, making it possible to configure IMA groups, add and delete links, and maintain IMA sublayer statistics.

PHY Layer Considerations

A typical PHY layer implementation with IMA is shown in Figure 2. In many such implementations, the Physical Layer function is resident on a "line card" which is physically separate from the ATM layer device to allow the ATM device to serve many facilities. This co-location of IMA on the line card restricts the facilities which can be allocated to an IMA group because only the specific T1 or E1 facilities attached to that line card can be grouped, limiting the configurability of the system.

One solution, for maximum configurability, is to place the IMA function with the ATM layer device. But this is usually difficult to implement and causes some system-level functional partitioning problems (such as splitting up the PHY layer across modules). A more common solution that sacrifices some of the flexibility in assigning facilities to IMA groups is to develop the IMA functionality and the line card so that each T1/E1 facility can be independently configured to be part of an IMA group or be bypassed around the IMA function to be accessed uniquely by the ATM layer device. With this solution, the line card is no longer a "dedicated" IMA card.

IMA Solution

Given the availability of many off-the-shelf devices providing the T1/E1 line interface, framing, and ATM Transmission Convergence (TC) sublayer functionality plus the wide acceptance and usage of the ATM Forum's UTOPIA bus interface for ATM cell transfer, it is natural to define an IMA solution that can be inserted between the TC function and ATM layer. With the availability of the Spartan-II family, a complete IMA solution can be implemented using a single XC2S150 device, an external SRAM device, and a software driver.

The IMA-8 Core

The IMA-8 product is an XC2S150 device solution that supports up to eight links and four IMA groups. The external interfaces for this FPGA device are shown in Figure 3. The IMA

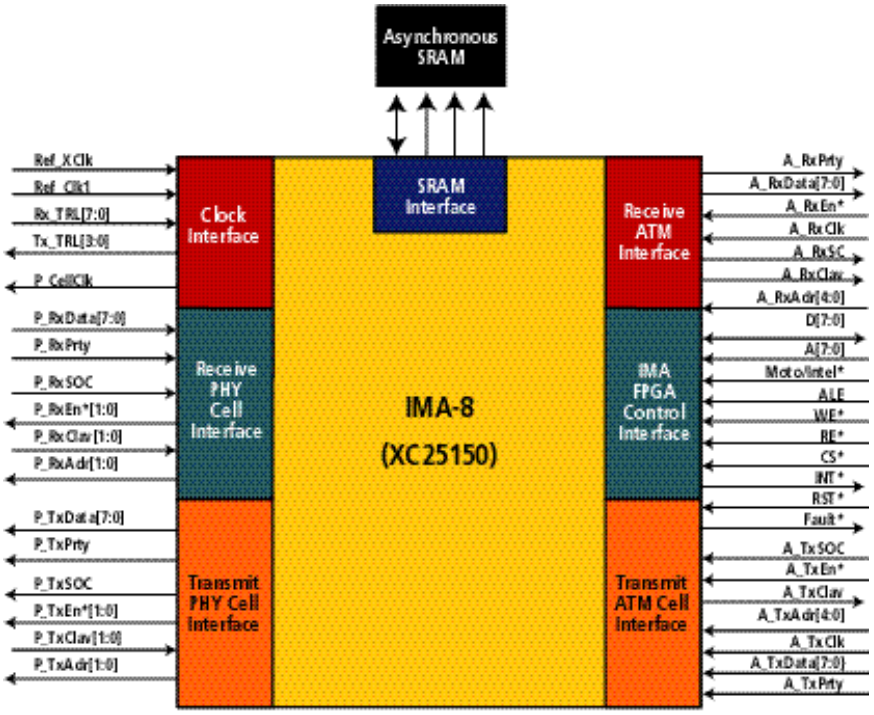

Figure 3 - IMA-8 interfaces.

implementation has been partitioned so the real-time processes are performed in the FPGA and all non-real time processes are performed by a software driver. For example, all IMA link state machines are implemented in the FPGA but the IMA group state machines are implemented in soft-ware. This partitioning eliminates interrupts from the FPGA and allows the software to operate as a periodic background task on the processor.

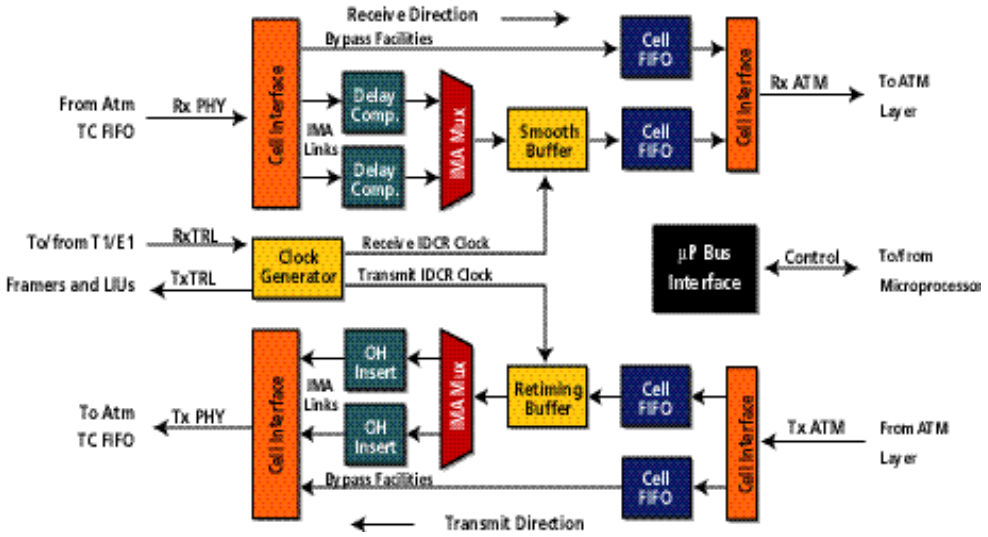

Figure 4 - Functional block diagram.

Functional Description

A simplified block diagram of the IMA FPGA solution is shown in Figure 4. The solution is composed of four main functional areas:

1 - the IMA clock generators.

2 - the Transmit IMA processing.

3 - the Receive IMA processing.

4 - the Microprocessor Bus Interface.

An IMA software driver completes the IMA implementation. To get specific details on these components, please contact Applied Telecom or the Xilinx High Volume Business Unit.

Conclusion

Early deployment of IMA technology meeting the IMA v1.0 standard began in late 1997, but due to different interpretations of this specification, true multi-vendor interoperability was not really possible until the completion and acceptance of the IMA v1.1 specification in 1999. Throughout this period, the changes to the applicable technical standard and the lessons learned through inter-vendor testing required the flexibility of FPGA and software implementations.

At present, stability in standardization plus large scale IMA deployment have set the stage for the introduction of standard silicon IMA products. But IMA is still an emerging technology with limited test equipment support and compliance test suites. An FPGA based IMA solution with efficient partitioning of hardware and software functions provides the necessary scalability and flexibility to handle all of these applications and allow for tracking of new standards.

With the introduction of the Spartan-II FPGA family and the IMA8L core (along with other Xilinx-based IMA core solutions) an FPGA based IMA implementation is simple and economical. Σ

The IMA-8 core is available immediately for use in Spartan-II FPGAs. An evaluation board and the DRV-IMA software are also available now. All IMA products can be purchased directly from Applied Telecom.See www.apptel.com.