The New XPLA3 CPLD Family

The Best CoolRunner Family Yet

CoolRunner devices are ideal for low-power, high-perfor mance applications.

by Reno Sanchez, CoolRunner Marketing & Applications Manager, Xilinx, renos@Xilinx.com

The CoolRunner™ CPLD families are the world's only CPLDs using the patented Fast Zero Power (FZP) design technique to simultaneously deliver high performance and low power consumption. These devices offer pin-to-pin (TPD) delays of 5.0 ns (or greater than 250 MHz system operation), and less than 100 uA of standby current (approximately 1/3 of the power consumed by all other competing CPLDs at FMAX).

These characteristics make CoolRunner devices ideal for low power applications that include portable, handheld, and power-sensitive applications. These devices are also idea for systems that have a strict power or thermal budget, a need for increased system reliability (less power means less activation energy and lower FIT rates), a need for lower cost (by eliminating or reducing the system cooling requirements), or a need for reduced power supply requirements (or battery operation). Figure 1 illustrates the CoolRunner CPLD families.

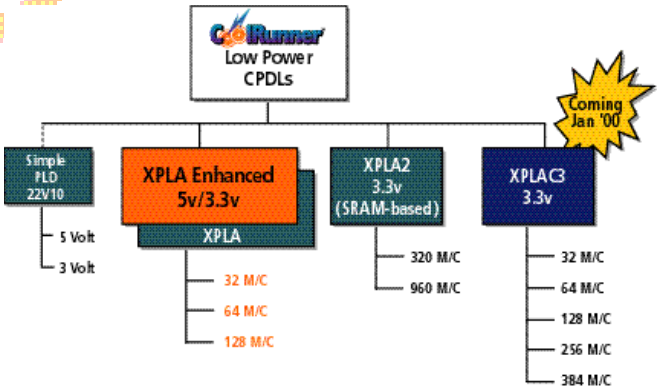

Figure 1 - CoolRunner CPLD family.

The XPLA3 Family

The XPLA3™ (eXtended Programmable Logic Array) is the newest CoolRunner CPLD family, and includes devices ranging from 32 to 384 macrocells. XPLA3 was created to maintain the same competitive advantages as the existing CoolRunner families, add additional features, and increase performance, while delivering all this at a substantially lower cost.

XPLA3 Architecture

The XPLA3 architecture is based on a PLA (Programmable Logic Array). The PLA is a programmable AND Array combined with a programmable OR Array. All other competing CPLDs employ a PAL (Programmable Array Logic) that combines a programmable AND Array with a fixed OR Array. Having a programmable OR Array allows product terms (PTs) to be shared between macrocells (effectively increasing design density because there is no duplication of logic), excellent pin locking (every PT is available

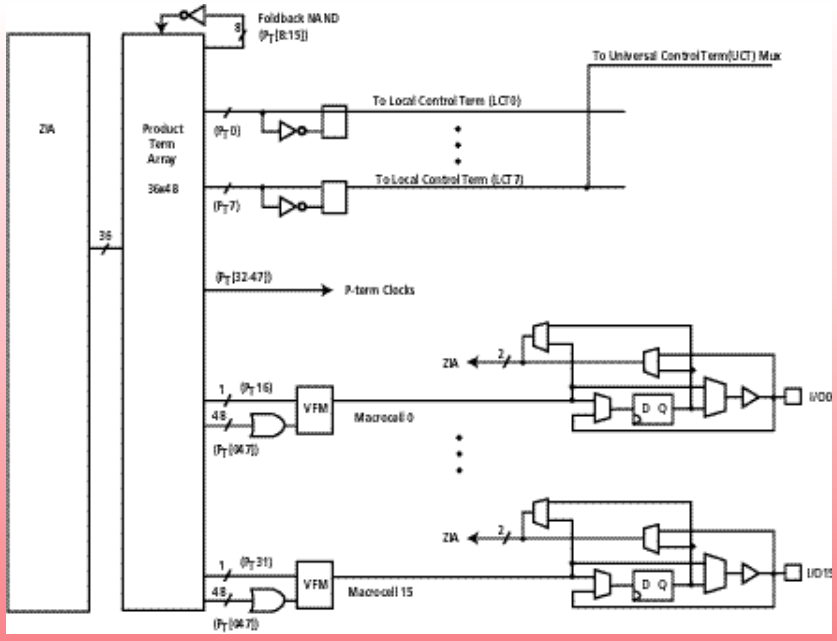

Figure 2 - XPLA3 Logic Block architecture.

to every macrocell), and very simple timing model (timing remains the same regardless of how many PTs are used).

The XPLA3 architecture includes a pool of 48 product terms that can be allocated to any output in the logic block, a direct input register path, multiple clocks (both dedicated and product term generated), and both reset and preset for each macrocell.

Figure 2 illustrates the logic block architecture. Each logic block contains control terms, clock terms, PLA array, and 16 macrocells. There are 36 pairs of True and Complement inputs from the ZIA that feed the programmable OR array. In addition there are 8 foldback PTs that are available for ease of fitting and pin retention. Also within the 48 p-terms there are eight local control terms (LCT 0-7) available as control inputs to each macrocell for use as asynchronous clocks, resets, presets, and output enables. The other PTs serve as additional single inputs into each macrocell. Sixteen of these are coupled with the associated programmable OR gate into the VFM (Variable Function Multiplexer). The VFM increases logic optimization by implementing any of the OR, XOR, XNOR, or NOR functions before entering the macrocell.

Each macrocell can support combinatorial or registered inputs; a global preset and reset for each macrocell; and configurable D, T, or L registers, with maximum clocking flexibility. Each of these flip-flops can be clocked from any one of nine sources. There are two global synchronous clocks that are derived from the four external clock pins via a four-to-two multiplexer. There is also one universal clock signal sourced by a global control term. The clock input signals LCT4-LCT7 (Local Control Terms) can be individually configured as either a product term or sum term equation created from the 36 signals available inside the logic block.

Conclusion

The XPLA3 CoolRunner CPLD family simultaneously delivers both high performance and low power consumption at a very competitive price, and will be the lead CoolRunner CPLD family for Xilinx in 2000.