Get the Best Registered I/O Timing with Virtex-E FPGAs

You can achieve I/O setup times of less than 1.6 ns, and I/O clock-to-out times of less than 3.3 ns, using LVTTL switching levels.

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Virtex-E FPGAs contain a number of architectural features that enhance I/O timing. Four dedicated clock buffer networks allow low skew distribution of clocks to a large number of loads, while guaranteeing zero hold time requirements between registers. You can also use on-chip clock Delay Lock Loops (DLLs) to effectively eliminate the phase difference between a clock external to the FPGA and the internally buffered equivalent. Plus, each Virtex-E I/O block (IOB) contains both an input an output register, which can be used to improve I/O timing.

The setup time for a signal brought on chip is the sum of the I/O pad delay, any routing and logic delays, and the intrinsic setup time of the register or latch, minus any clock delay. Clock delay is the sum of I/O pad delay, any clock buffer delay, plus routing and loading delays. Of these items, only the I/O pad delays and register setup times are known precisely. All other factors are design dependent. Clock-to-out times require similar calculations, except that any clock delay worsens the clock-to-out time.

Registering Input Signals

Based on your system timing requirements you can allocate a setup time, hold time, and clock-to-out timing budget for the Virtex-E device. Typically, you are looking for the minimum required setup time for the FPGA, and zero (or negative) hold time.

The system-level timing specification references all input signal and clock timing values to the pins of the FPGA device. For example, a 5ns setup time budget means:

- Valid data will exist at the FPGA pin a minimum of 5ns prior to an active clock edge at the pin of the FPGA.
- The timing at the FPGA register used to capture this input signal must meet its own setup and hold time requirements.

It is mandatory that both of these requirements be met within the overall system timing budget.

You can alter input timing when using Virtex-E chips by controlling the following choices:

Selection of IOB and CLB

In Virtex-E FPGAs, input signal registers can be located in either IOBs or in CLBs. An advantage of using an IOB register is that the data path delay (consisting of I/O pad and buffer delays, plus routing) is fixed. If a CLB register is used, the routing delay will vary depending upon where the CLB is placed, and the routing path taken.

Using the appropriate timespecs can improve the setup timing when using CLB registers, but will not cause the Alliance Series™ or Foundation Series 2.1i software to move registered signals between IOB or CLB registers. If the source netlist contains register components with the property IOB = TRUE, these will not be moved. However, by either setting a MAP command line switch (map -pr i) or through enabling a GUI-based option to allow MAP to pack registers into the IOB cells, then a netlist which did not contain IOB registers can use IOB registers if possible.

Using DLLs

If a clock is distributed using a global buffer only (not a clock DLL) there is a delay between the clock at the FPGA input pin and the clock internal to the FPGA. This delay is beneficial in that it reduces the required setup time for the input signal. If a clock DLL is used, the propagation delay is effectively zero, and the equivalent system setup time is increased. This apparent disadvantage of using a clock DLL is offset by removal of the delay element (described in the next paragraph), and the improvement in clock-to-out times.

Using or Eliminating the IOB Delay Element

By default, a delay element is placed in the data path of the IOB. This delay block is used to guarantee a zero hold time for the IOB register, but has the effect of increasing the required setup time. If a clock DLL output is not used as the I/O register clock, and the delay element is removed, the setup time required will decrease dramatically, but now a positive hold time exists.

If you use a clock DLL, the delay element can safely be removed, giving you the dual benefit of less required setup time and a negative hold time. Beginning with the Alliance Series and Foundation Series 2.1i Service Pack Number 2, the delay element is included only when a DLL is not used and an IOB input register is used. This default behavior was changed from earlier software versions.

Registering Output Signals

When you are driving a registered signal off chip, you must meet a system clock-to-output specification. Fortunately, you have a number of simple options that can be used to meet this timing when using Virtex-E devices. The choices include:

Using IOB or CLB registers

You can choose whether the output register is an IOB register or a CLB register. The IOB register will always have a shorter routing path from register output to FPGA pin, so the fastest clock-to-out time will always be achieved by using the IOB register. Timespecs alone will not force the Alliance Series or Foundation Series 2.1i software to make the register type decision. However, by either setting a MAP command line switch (map -pr o) or through enabling a GUI based option to allow MAP to pack registers into the IOB cells, IOB output registers will be used, if possible.

	Run #1 Baseline	Run #2 Timespecs	Run #3 Add Pack IOB Registers	Run #4 Add NODELAY	Run #5 Add Fast Slew	Run #6 Add24 ma Drive	Run #7 Pick Best Results
Tsu (no DLL)	0.906 ns	0.442 ns	1.795 ns	-0.403 ns	-0.403 ns	-0.403 ns	1.795 ns
Tc2o (no DLL)	8.934 ns	9.082 ns	6.554 ns	6.554 ns	4.654 ns	4.453 ns	4.453 ns
Tsu (DLL)	2.407 ns	2.214 ns	1.555 ns	1.555 ns	1.555 ns	1.555 ns	1.555 ns
Tc2o (DLL)	7.837 ns	7.924 ns	5.325 ns	5.325 ns	3.425 ns	3.224 ns	3.224 ns

* The gray shading indicates a positive hold time requirement.

Table 1 - Runtime results.

Using Clock DLLs

Any delay of the input clock due to clock buffer and clock routing delays adversely effect clock-to-out timing, because this delay simply adds to the overall datapath delay. The use of a clock DLL will always result in faster clock-to-out times in a Virtex-E FPGA.

Using Slew Rate and Drive Strength Options for LVTTL Outputs

If LVTTL output buffers are selected, you can choose between seven drive strengths, and between fast and slow slew rate. By default, a Virtex-E output buffer defaults to LVTTL, 12ma drive, and slow slew rate. To improve clock-to-out times, select a higher drive strength (16ma or 24ma) and fast slew rate. The place and route software will not modify output buffer settings to meet a timespec; you must do this explicitly, typically by using a constraint file.

Summary of Recommendations

- Use IOB input and output registers when possible.
- Use clock DLLs when possible.
- Set fast slew rate and 24ma drive for LVTTL I/O to get fastest clock-to-out times.
- Set NODELAY mode when using clock DLLs to get shortest setup time.
- If clock DLLs are not used, NODELAY will greatly shorten your setup time, at the cost of a positive hold time.

Xilinx created a simple design to demonstrate the effects discussed above. The results are shown below.

Test Results

In Table 1 Run #1 shows the registered I/O timings using default settings and CLB registers. By adding timespecs (5ns setup, 10ns clock-to-out), results changed slightly (Run #2). Packing registers into IOBs (Run #3) gives a better clock-to-out delay, and a slightly worse setup time. The timing effects of setting NODELAY (Run #4), plus fast slew rate (Run #5), plus high drive (Run #6) are shown. Finally Run #7 gives the best results with zero hold time in all cases.

Conclusion

With new Virtex-E family you can easily achieve very fast registered I/O timing.

For complete information on Virtex-E FPGAs, see www.xilinx.com.