IMAGE COMPRESSION CORE

For Virtex-E and Spartan II FPGAs

These new cores target JPEG, MPEG, DSP, and image processing applications.

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Xilinx and Xentec recently announced new AllianceCORE products for Image processing. These cores include a discrete/inverse discrete cosine transform (DCT and IDCT) and a JPEG codec. The DCT/IDCT core supports Virtex, Virtex-E, and Spartan-II devices, and is a critical building block in Dolby AC2 and AC3, JPEG, and MPEG compression systems. The JPEG codec supports Virtex and Virtex-E devices, and provides a fully integrated encoder-decoder pair used in image compression and decompression applications.

Target applications for the new cores include image storage, data and video compression, medical imaging, and industrial systems. Xentec developed these very compact image compression cores by using the versatile DSP features in the Spartan-II and Virtex architectures.

DCT and IDCT Solution in a $10 FPGA

The DCT/IDCT core enables high-speed hardware implementation of the forward and inverse discrete cosine transform functions. DCT and IDCT (Inverse DCT) functions are the building blocks of JPEG, MPEG, and ITU-T H261 standards-based codecs that are used in many image processing applications.

A DCT function is a key element in a compression system that splits still-image pixels into smaller data blocks. It calculates a value to represent each block that can be used to reduce the storage space required for the overall image. The IDCT function operates in reverse and reconstructs the image from compressed data.

Xentec's DCT/IDCT core performs both DCT and IDCT functions and is ideally suited for systems that require both image compression and decompression. It supports both DCT and IDCT on 8x8 image pixel data. DCT or IDCT mode is selected by means of a control signal. The core fits in a single XC2S100 Spartan-II FPGA that costs just $10 in high volume.

"Digital imaging applications typically need the power of 32-bit processors for implementing the computationally intensive DCT/IDCT functions in software," said Robert Bielby, Xilinx Director of Strategic Applications. "By moving the DCT/IDCT function into a cost-effective

Spartan-II device, designers can now use cheaper eight-bit microcontrollers and cut down the overall system costs."

Integrated JPEG Codec Solution

JPEG is an image compression technique for reducing image file sizes without a noticeable difference in image quality. The Xentec X_JPEG codec core conforms to the ISO/IEC 10918-1 JPEG baseline specification and performs both compression and decompression functions. The full-featured core includes support for stalling and the ability to handle four-color components. It is extremely flexible, including four programmable quantization and four programmable Huffman tables that allow you to specify quantization, Huffman table, and the quantity of pixel blocks assigned for each color component.

"The memory hierarchy in the Xilinx Virtex-E FPGAs enabled us to develop an extremely small JPEG core," said Xerxes Wania, President and CEO of Xentec. "We used distributed SelectRAM™ to build ROM-based Huffman tables that are distributed across the design and embedded block SelectRAM for the large DCT/IDCT, quantization, and zig-zag coding tables. The end result is a flexible, optimized codec solution that includes both logic and memory in a single medium-density FPGA."

Spartan-II FPGAs

The Spartan-II family delivers 100,000 system gates for under $10 at speeds of 200 MHz and beyond, and provides unmatched design flexibility. These low-power 2.5-volt devices feature I/Os that operate at 3.3 volts with full 5-volt tolerance. Spartan-II devices also feature multiple Delay Locked Loops (DLLs), on-chip RAM (block and distributed), and the versatility of SelectI/O™ technology supporting over 16 high-performance interface standards, in a device that offers unlimited programmability and can be upgraded in the field.

Virtex-E FPGAs

The Virtex-E family has made significant improvements in the areas of capacity and performance over the original Virtex series. The family features devices with 3.2 million gates, 832 Kbits of True Dual-Port internal block RAM, eight digital Delay Locked Loops (DLLs) capable of over 300 MHz clock frequency for system timing, and three new differential signal standards. The Virtex-E FPGAs are the first programmable logic devices delivered on 0.18-micron process technology, which Xilinx jointly produced with Taiwan's UMC Group. The improved process directly contributes to the 30 percent performance gain for all internal functionality. Also, the Virtex-E family represents the industry's first programmable logic architecture with 210 million transistors on a single device.

Availability and Pricing

The X_JPEG and X_DCT_IDCT cores are immediately available from Xentec, Inc. The DCT and IDCT core is available for use in Spartan-II, Virtex-E, and Virtex FPGAs, and lists at $10,000 for the netlist version. The JPEG codec is available for use in Virtex-E and Virtex FPGAs, and lists at $30,000 for the netlist version. All Xentec products can be purchased directly from Xentec. The datasheets can be downloaded from the Xilinx IP Center (www.xilinx.com/ipcenter), a comprehensive resource for system-level intellectual property and services.

Conclusion

Xilinx FPGAs, along with the Xentec cores, provide a complete solution for creating image processing applications. This combination helps you quickly get your products to market, saving you time and money. Σ