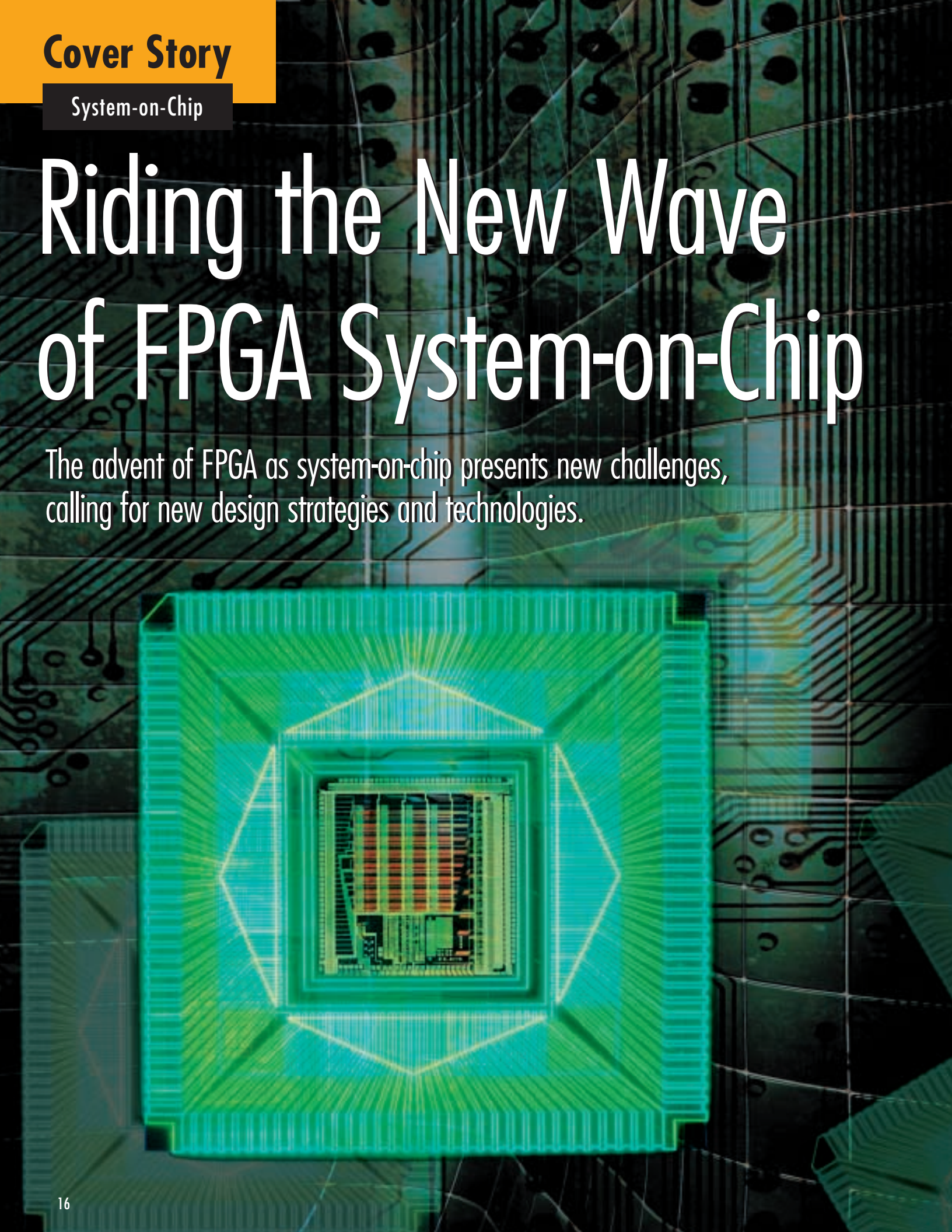
Riding the New Wave of FPGA System-on-Chip

The advent of FPGA as system-on-chip presents new challenges, calling for new design strategies and technologies.



by Anne Sanquini
VP & General Manager, HDL Design Division, Mentor Graphics
anne_sanquini@mentor.com

Adoption and assimilation have always been the modus operandi for successful, lasting conquest. We are witnessing the advance of FPGAs (Field Programmable Gate Arrays) against ASICs (Application Specific Integrated Circuits) in terms of performance, complexity, size, and revenue. The unfamiliar challenges and frustrations that FPGA designers are beginning to face are not new to the ASIC world, as manifested in SoC (System-on-Chip) design. Ten-million-gate platform devices call for a complete design environment, not just one that borrows from the ASIC world, but one designed with knowledge of and explicitly for the FPGA world.

ASIC vs. FPGA - Not Your Grandmother's FPGA

The FPGA market has undergone an interesting revolution. As FPGAs have improved in terms of speed, volume, and size, programmable logic silicon has cut deeper into the ASIC market. The performance, complexity, and density gap is closing, and FPGAs enjoy lower development costs, while those of ASICs continue to rise.

Plus, unless you're building as many as 50,000 or 100,000 units a year, you're probably better off going to production with an FPGA. Because you can customize an FPGA, you don't have to spend time "in the fab" (in the fabrication process). The results are significant cost savings and much faster time to market.

FPGA - The Darling of Fab

Another relevant development is the takeover of semiconductor manufacturing by specialty fab houses. In the past, FPGAs lagged behind ASICs in performance and density because FPGAs were not welcomed in the fab houses owned and operated by the big semiconductor companies. These internal fabrication operations favored high volume, uniform chips like DRAMs – chips that run over and over again without changing. Therefore, companies didn't put the energy and resources into developing FPGAs.

That's all changed. FPGAs are now the leading-edge semiconductor process technology drivers. New fab foundries have replaced DRAMS with FPGAs as their process drivers, because identical FPGAs can be run in very high volumes – unlike most ASICs. FPGAs, by definition, are programmable by the customer. Now, through partnerships with fab houses, Xilinx has their semiconductors built directly for them. For these and other reasons, FPGAs are an increasingly valuable technology, providing liberating flexibility at a low cost.

The Price of Success – The Challenge of the Ten-Million-Gate Platform Device

The rapidly evolving FPGA market will continue to erode the ASIC market, not only because of programmable logic's traditional advantages, but also because of its greater capabilities – potential and actual. FPGAs are getting bigger, faster, and richer in functionality. This is important for improving ASIC prototyping, yet it also drives the migration of FPGA to SoC.

The competitive advantage of FPGA SoCs has arrived. Today, close to 50% of FPGA designs are SoCs. That means you'll be running up against SoC issues. The combination of large, complex IP (Intellectual Property) blocks and embedded software,

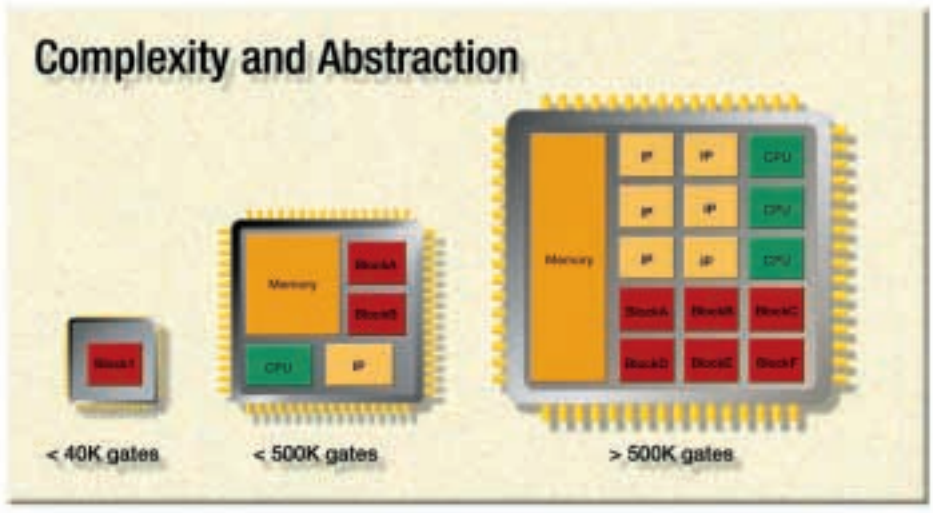


Figure 1 - The increasing density, higher speeds, and application of mixed design with IP cores has enabled the new FPGA/SoC environment.

combined with soaring transistor count, tax the capabilities of traditional design methodologies – particularly verification tasks, which now can consume 60% to 80% of design resources. The high densities, small geometries, and increased role of interconnects in device behavior present daunting challenges during synthesis.

Historically, FPGAs were small devices, so FPGA designers were able to experiment with various programming options until they got it right. Yet, as FPGAs have increased in density and performance, they've become too large for ad hoc design. The time cost of just figuring out where the bugs are has become too great.

Today's FPGAs cause problems for ASIC and board designers as well, who now have to deal with high pin counts and high frequencies on their boards. In the past, FPGAs were considered just bits of programmable logic board designers could use to sweep up the stuff on the PCB that they forgot to put in their ASICs. All of that has changed by what Xilinx has done to improve FPGA functionality. Board designers can be overwhelmed by this "new" FPGA technology.

The challenges of SoC call for designs that take advantage of high production runs, accommodate fast debug and verification, adapt to changing standards, work with both IP cores and custom logic, and meet rigorous performance requirements. Designers demand tools that provide high QoR (Quality of Results) for their FPGAs, optimize their entire design at once in a top-down design flow, enable aggressive optimization of individual design blocks, and provide tight integration with vendor IP tools. Meeting all of these requirements while still getting to market quickly begs for team design. Designs are simply too big and complex for a single designer. Team design is supported by an incremental, modular approach that implements design reuse effectively. Modular design – combined with physical optimization – support the need for large high-performance designs, shorter design cycles, and a team-based approach.

Along with design complexity, verification is emerging as a critical design strategy. The focus has shifted from content creation to the problems of evaluating, integrating, and verifying multiple pre-existing blocks and software components. This methodology is characterized by more in-depth system-level design, concurrent hardware/software design and verification, and verification at all levels of the design process.

Turning Silicon into Gold

FPGA designers must be able to handle and manage the enormous amount of data required for today's FPGAs. What's important is that whether you're an FPGA designer stepping up to the next level, or a board designer challenged with new FPGA devices, your tools must talk to each other. Integration is key. And the tools must be available for both FPGA and PCB designers.

You'll need an FPGA flow that provides a high QoR for faster devices and a synthesis flow that provides control over the design. You will want a complete flow that works with design creation and simulation. Furthermore, you'll need a flow that easily mixes legacy design with memory and IP. Finally, you'll look for the ability to quickly and easily insert IP cores from FPGA vendors and third parties.

Mentor Graphics has a history of expertise and investment in this kind of comprehensive, interlocking solution – in this case, a comprehensive set of FPGA development tools. Conversely, many EDA (Electronic Design Automation) companies are blind to what is going on with FPGAs. Their tools are tuned toward ASIC design. FPGA cus-

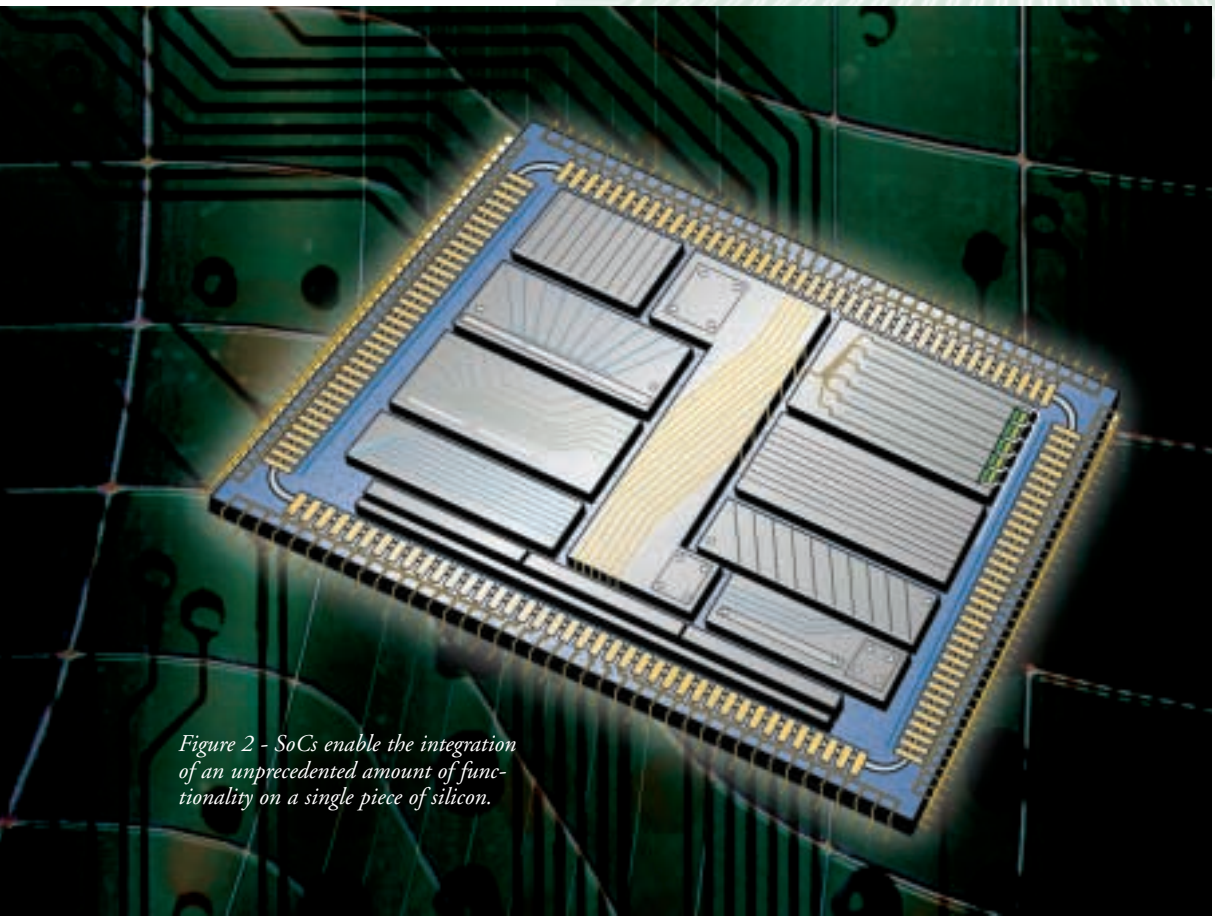


Figure 2 - SoCs enable the integration of an unprecedented amount of functionality on a single piece of silicon.

tomers are at a disadvantage, because to come up with the same solution, these ASIC-centric companies would have to turn their focus to another set of issues – issues faced specifically by the FPGA designer. For various reasons, they're reluctant to do that.

A Complete, Interwoven Design Flow

Mentor Graphics is a leader in SoC design tools and design productivity solutions. In addition, the company has concentrated on and invested in FPGA technology. We're positioned to help FPGA design teams succeed by offering a complete tool suite for the entire FPGA design flow – from creation through simulation to synthesis – with FPGA Advantage™.

Mentor's LeonardoSpectrum™, the world's number one FPGA synthesis tool, provides physical integration for modular design and IP integration for design reuse. LeonardoSpectrum delivers high QoR for the latest FPGAs, optimizes the entire design at once in a top-down design flow, enables aggressive optimization of individual design blocks, and provides tight integration with vendor IP tools. Meanwhile, Mentor's TimeCloser™ technology provides physical optimization and bi-directional integration with the Xilinx place-and-route tools to help achieve desired performance levels.

The increased impact of debugging on design productivity means that designers need tools that allow them to rapidly create, modify, debug, and document sophisticated HDL designs using real-time syntax and semantic verification. FPGA Advantage enables both easy detection of bugs and quick design modifications. This solution also supports design reuse and team design. With hardware and software IP available through the Mentor Graphics Inventra™ IP cores and VRTXoc Real-Time Executive™, Mentor Graphics further supports the time-to-market and design productivity advantages of design reuse.

A multi-tiered verification methodology that takes full advantage of early-design simulation techniques enables concurrent hardware/software verification and minimizes dependence upon late-design verification. Seamless™ – the leading hardware/software co-verification tool – delivers hardware/software interface verification capabilities extensively and consistently throughout the design process.

Successful SoC design also requires a proven, reliable simulation environment supporting simulation at all levels of the design flow. Through functional and timing simulation, ModelSim™ and the industry-standard XRAY® Debugger provide verification at the chip level. Verification at the system level is handled by Tau™, utilizing STAMP models for board-level static timing analysis, and the ICX™ tools, which apply IBIS™ models for signal integrity analysis.

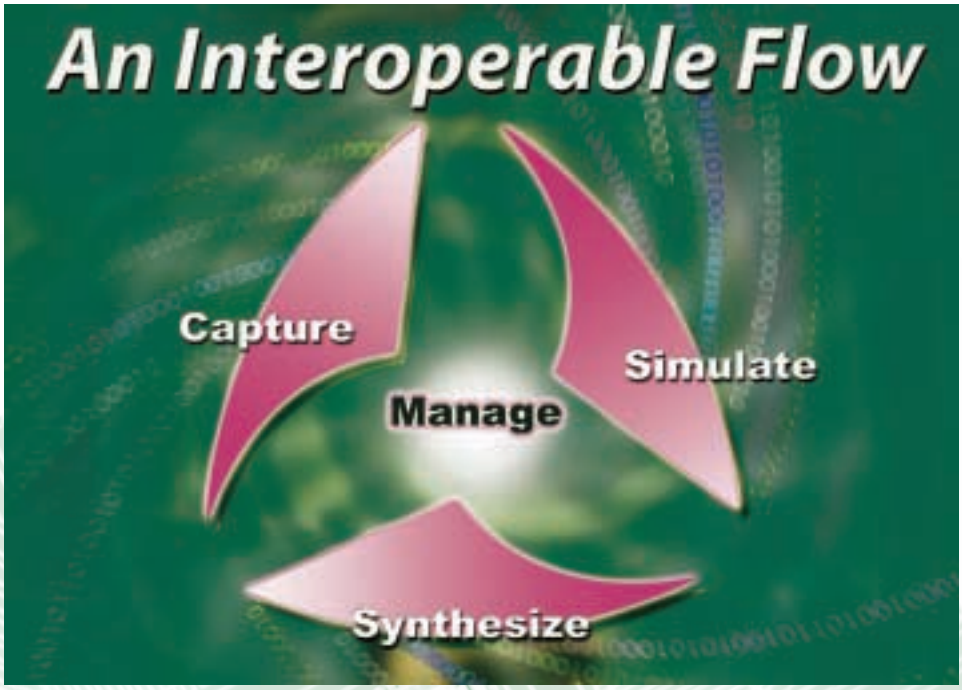


Figure 3 - The team-based approach required by today's FPGA designs are best supported by a single, integrated design solution.

Single Vendor Design Flow

Mentor Graphics offers a tested, integrated solution that works for both FPGAs and SoCs, all from one company. FPGA designers are already discovering that working with a single development tools provider is both convenient and efficacious. Plus, by design, the Mentor Graphics EDA tools can be integrated with third-party products and IP. Mentor Graphics FPGA design tools are language and platform neutral because design teams need the ability to work in VHDL, Verilog, and mixed-language environments, as well as on UNIX and Windows-based platforms. Mentor Graphics is unique in the industry in that we can deal with both the embedded software customer – through our Embedded Software Design division – and the FPGA customer with our FPGA Advantage flow. Nobody else has that flow, in terms of tightness, completeness, and relevance to those specific customers.

As FPGAs have become more complex, Mentor Graphics has been well positioned to step in with the appropriate design solutions. Our complete design flow gains its integrity from advanced features for FPGA SoC creation, including incremental synthesis and modular design, leading device support, integration with vendor IP flows, and flexible design flows for million gate designs. Together, Mentor and Xilinx plan to speed the adoption of FPGAs because the benefits and opportunities are enormous.