Save Prime PCB Real Estate with Chip Scale Packaging

With innovative chip scale packaging, Xilinx CPLDs provide high speed, low power, and design density solutions.

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Size does matter when it comes to designing for space sensitive applications such as personal electronic equipment. As the industry leader in advanced packaging technology, Xilinx sells CPLDs (Complex Programmable Logic Devices) in CSPs (Chip Scale Packages) at competitive cost points. Xilinx was the first company in the programmable logic industry to offer CSPs in 0.8 mm BGA (Ball Grid Array) spacing (pitch) with the 9500 series of CPLDs. Now, Xilinx also offers 0.5 mm BGA spacing with the CoolRunner™ XPLA3 devices. These inexpensive CPLDs further decrease system costs by minimizing the amount of PCB (Printed Circuit Board) space and total system packaging required for any solution.

Because of the expensive nature of multiple layer, high speed digital PCBs, chip scale CPLDs provide cost-reduced solutions by consuming less real estate for any application, regardless of size. Consider the replacement of a 44-pin PLCC (Plastic Leadless Chip Carrier) package (PC44) by a 56-ball CSP with a 0.5 mm pitch (CP56). The CP56 solution requires only 11% of the space previously occupied by the PLCC package (Figure 1). Moreover, the CP56 provides 33% more user I/Os. (Ed. note: The CP56 has 48 user I/Os, and the PC44 has 36 user I/Os - thus, 33%.) Finally, CSPs offer reduced chip-to-chip delays (because the devices can be placed closer together), increased thermal performance, and higher reliability.

Mount 'Em Up!

Designing PCBs for BGA packages requires a slightly different technique than typical surface mount components, but most PCB designers can learn the technique easily. Many pad geometries are used in the design and application of CSP solutions, from circular to diamond shaped mounting pads.

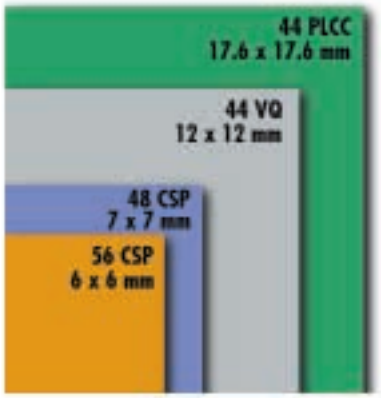

Figure 1 - A 56 CSP (CP56) occupies 11% of the space of a 44 PLCC and offers 33% more I/Os.

The circular pad is the preferred mounting method employed by most PCB designers today. Geometry details will be briefly provided here, but for additional information, obtain PDF copies of XAPP157 "Board Routability Guidelines with Xilinx Fine Pitch BGA Packages" (www.xilinx.com/xapp/xapp157.pdf) and Virtex Tech Topic "Xilinx Fine-Pitch BGA and CSP Packages: The Technological Edge" (www.xilinx.com/products/virtex/techtopic/bga_csp.pdf).

BGA packages come in two types of surface mount pads: SMD (Solder Mask Defined) and NSMD (Non Solder Mask Defined). As the names imply, these describe the way the copper is revealed on the surface of the PCB for solder attachment to the BGA package. SMD pads have portions of solder mask overlapping the pad; NSMD pads have an annulus of space around the perimeter of the pad (Figure 2).

Figure 2 - Cross section of SMD and NSMD pads

Xilinx recommends using NSMD pads be used. For a brief summary of the dimensions of the pads, refer to Table1. A note of cau-

Pitch (mm)	Package	NSMD Pad (mm)	Thru Via (mm)	Via Capture (mm)	Inner Trace (mm)	Outer Trace (mm)	Space (mm)
0.8	CS280	0.33	0.30	0.50	0.1	0.127	0.120 / 0.100
0.8	CS144	0.33	0.30	0.50	0.1	0.127	0.120 / 0.100
0.8	CS48	0.33	0.30	0.50	0.1	0.127	0.120 / 0.100
0.5	CP56	0.27	0.30	0.55	0.1	0.127	0.127

Table 1 - Basic pad and layout geometries

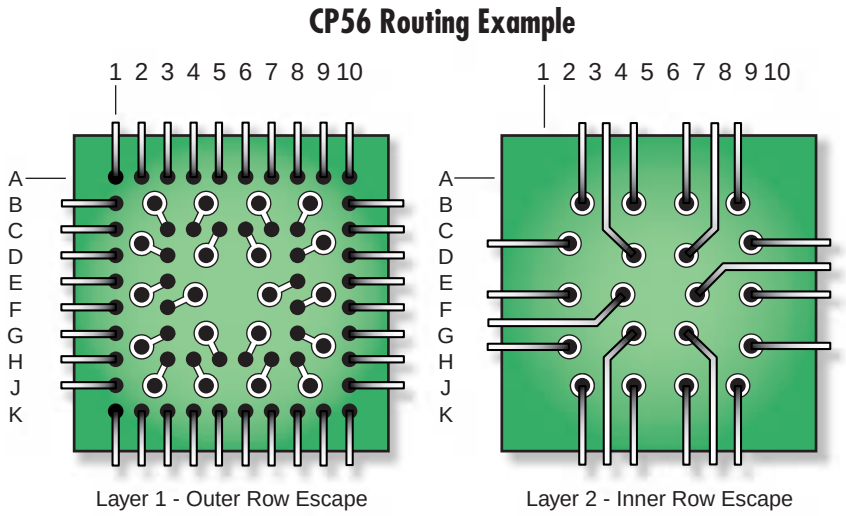

Figure 3 - 56-ball grid array in a chip scale package

tion: You should discuss the choice of the pad geometry, the width of the signal traces, and the solder mask/trace clearances with your PCB vendor to determine feasibility.

Escape to Higher Reliability

CSPs provide higher reliability and performance. Their ball grid packages provide superior bonding integrity in applications subjected to vibration, flex, and thermal fluctuations. Ball grid packages are self-aligning during the soldering process, and they are naturally immune to manufacturing issues such as pin non-coplanarity and other pin-related damage. When it comes to routing a CSP device, Xilinx provides an access and escape pattern that is easy to use. Because the I/O signals are placed on the outer ring of the ball grid pattern (power and ground are typically positioned inside), the escape pattern is simple and straightforward (Figure 3).

Don't Sweat the Heat

Due to the basic form factor of a BGA package, the solder balls mounted in a uniform array under the device help to dissipate heat from the CPLD and allow use of the PCB as a heat sink much more efficiently. Consider the 1.0mm quad flat package VQ44 volume (105 mm^3) compared with the CS48 package volume (66 mm^3) for the XC9536XL. Even though the CS48 device is significantly smaller than the VQ44 package (Figure 1), the thermal resistance of the CS48 is slightly less than the thermal resistance of the larger VQ44 package.

Refer to Table 2 for thermal resistances of some of the Xilinx CSP CPLD devices. Note that these values may be calculated rather than measured.

Using the thermal resistance (θ_{JA}) of a package to calculate junction temperature is quite simple. Thermal resistances are given in (C/W degrees Celsius per Watt) dissipated. For junction temperatures, multiply the thermal resistance by the amount of power (in watts) dissipated by the device, and add in the ambient temperature. Note, this is valid for calculations in still air. If forced air-cooling is used, other thermal resistance values are available that are applicable to a flow rate. These flow rate related thermal resistances and other temperature and package information can be found at www.xilinx.com/partinfo/databook.htm#packages.

Shrink Your Sockets, Not Your Options

As shown in Table 3, Xilinx already has almost a dozen CSP CPLDs in production, with plans to produce even more devices in space-saving chip scale packages. CSP CPLDs are being manufactured in both 0.8 mm (CS) and 0.5 mm (CP) ball grid spacing. Note the CS and CP designators (Figure 4) are used in the actual part numbers to designate package type. Refer to the device data sheets for information on creating the full part number.

Clearly, Xilinx CSP CPLDs are the product of choice for space conscious designers of personal and portable equipment. Just as clearly, they are the choice for engineers of any application requiring maximum performance, reliability, and cost efficiency under any conditions.

Figure 4 -CS (0.8mm) and CP (0.5mm) CSP pitch designators are stamped on the CPLDs.

Device	CP56	CS48	CS144	CS280
XCR3064XL	65°C / W			
XC9536		45°C / W		
XC9536XL		45°C / W		
XC9572XL		45°C / W		
XCR3128XL			34°C / W	
XC95144XL			34°C / W	
XC95144XV			34°C / W	
XCR3256XL				30.5°C / W
XC95288XL				30.5°C / W

Table 2 - Thermal resistances of some Xilinx CSP CPLD devices

CS48 7 mm X 7 mm (0.8 mm pitch)	CP56 6 mm X 6 mm (0.5 mm pitch)	CS144 12 mm X 12 mm (0.8 mm pitch)	CS280 16 mm X 16 mm (0.8 mm pitch)
XC9536	XCR3064XL	XC95144XL	XC95288XL
XC9536XL		XCR3128XL	XCR3256XL
XC9572XL			
XCR3032XL			
XCR3064XL			

Table 3 - Xilinx chip scale package CPLDs are being manufactured in both 0.8 mm (CS) and 0.5 mm (CP) ball grid spacing.