Synplicity Certify Software Integrates Xilinx ChipScope Debugging Tool

An easy to use graphical interface makes it simple to conduct data signal probes.

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Synplicity Certify™ 3.1 software now supports debug insertion for multiple FPGA-based ASIC prototypes via Xilinx ChipScope™ Tools. Figure 1 shows the current ChipScope usage model and which formerly manual steps are now handled automatically by Certify ASIC – prototyping software. ChipScope core generation – both ILA™ (Integrated Logic Analysis) and ICON™ (Integrated CONtrol) – and insertion are now automatic.

You can specify signals to be probed during or after partitioning. The procedure is similar to the current probe feature of the Certify software.

Figure 2 shows how ChipScope probes are organized into the Certify user interface. You can add ChipScope ICON cores to multiple FPGA configurations, but only one ICON core can exist per FPGA. The ICON core can have multiple ILA cores (up to a maximum of 15), and each ILA core can contain a set of signals to be probed (up to a maximum of 256 bits).

ILA cores can also have sections – one for the clock signal, one for the trigger signal(s), and one for the data signals (probed signals). The ILA core requires one clock signal, which must be related to the data being captured. When no unique trigger bus is specified, the data bus is used as the trigger. The data signals are the actual signal being probed. Dragging a signal into an ILA data signal section will enable its tracing through the ChipScope logic analyzer.

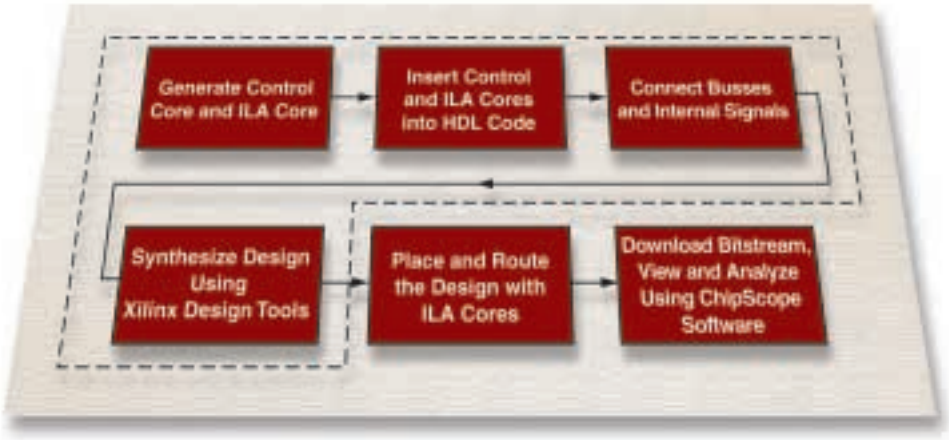

Figure 1 - ChipScope flow handled by Certify software

ChipScope Tools can generate and insert the ILA and ICON cores after all the partitioning is done. EDIF netlists will be created for each ILA and ICON core. They can be inserted into the design and connected using the information in the probe section of the partition information view. They can be marked as "black box," to be left untouched during the synthesis process. The EDIF files can be placed into the implementation directory.

By using the ChipScope integration with Synplicity Certify software, you can easily chose which signals to observe for debugging from an RTL (Register Transfer Level) view in an easy to use intuitive fashion.

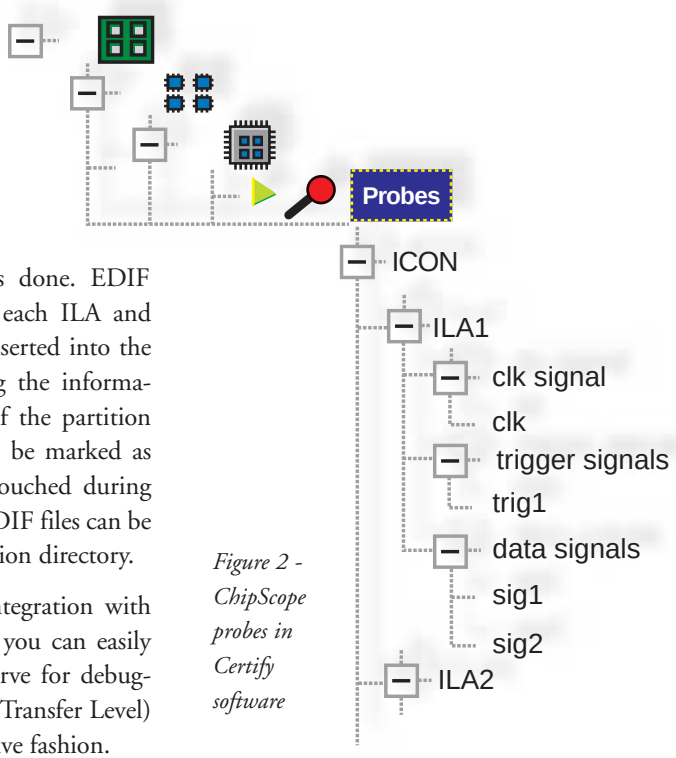

Figure 2 - ChipScope probes in Certify software