Build Scalable DSP Systems with Nallatech DIME Modules Populated by Virtex-E FPGAs

By their nature, FPGAs are ideal for DSP systems that must grow and evolve on demand.

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Today's digital signal processing systems often require significant performance and resources beyond the capability of traditional DSP processor-based architectures. FPGAs offer quick turnaround, high performance, and reconfigurable technology. Therefore, FPGAs are finding applications in HDTV, base stations, and other high-speed DSP communications systems because of their distinctive combination of performance and flexibility.

Even high-end DSP systems can benefit further from parallel FPGA architectures, which introduce scalability into your system architecture. Scalable systems must cope with high I/O and processing bandwidth requirements, dynamic configurations, and real world interfaces. Implementing parallel FPGA configurations from the outset ensures your DSP systems will meet future demands and maximize silicon performance. Traditional DSP processors just can't keep up.

High Speed DSP Development Platform

DIME™ (Dsp and Image processing Module for Enhanced fpgas) is an open modular standard from Nallatech Ltd. that provides the framework for a scalable systems approach, making it particularly suitable for high speed DSP applications. As shown in Figure 1, a fundamental example of a FIR/FFT (Finite Impulse Response/Fast Fourier Transform) processing combination demonstrates how DIME modules can be utilized to construct a multiple FPGA-based DSP system.

The system can be implemented on a Ballynuey2 DIME motherboard populated with two DIME modules – the Ballyriff and the BallyDAC. A high-level configuration tool for the Ballynuey2 carries out the configuration of the FPGA devices fitted to the two DIME modules and thus allows configuration of multiple FPGAs in a system.

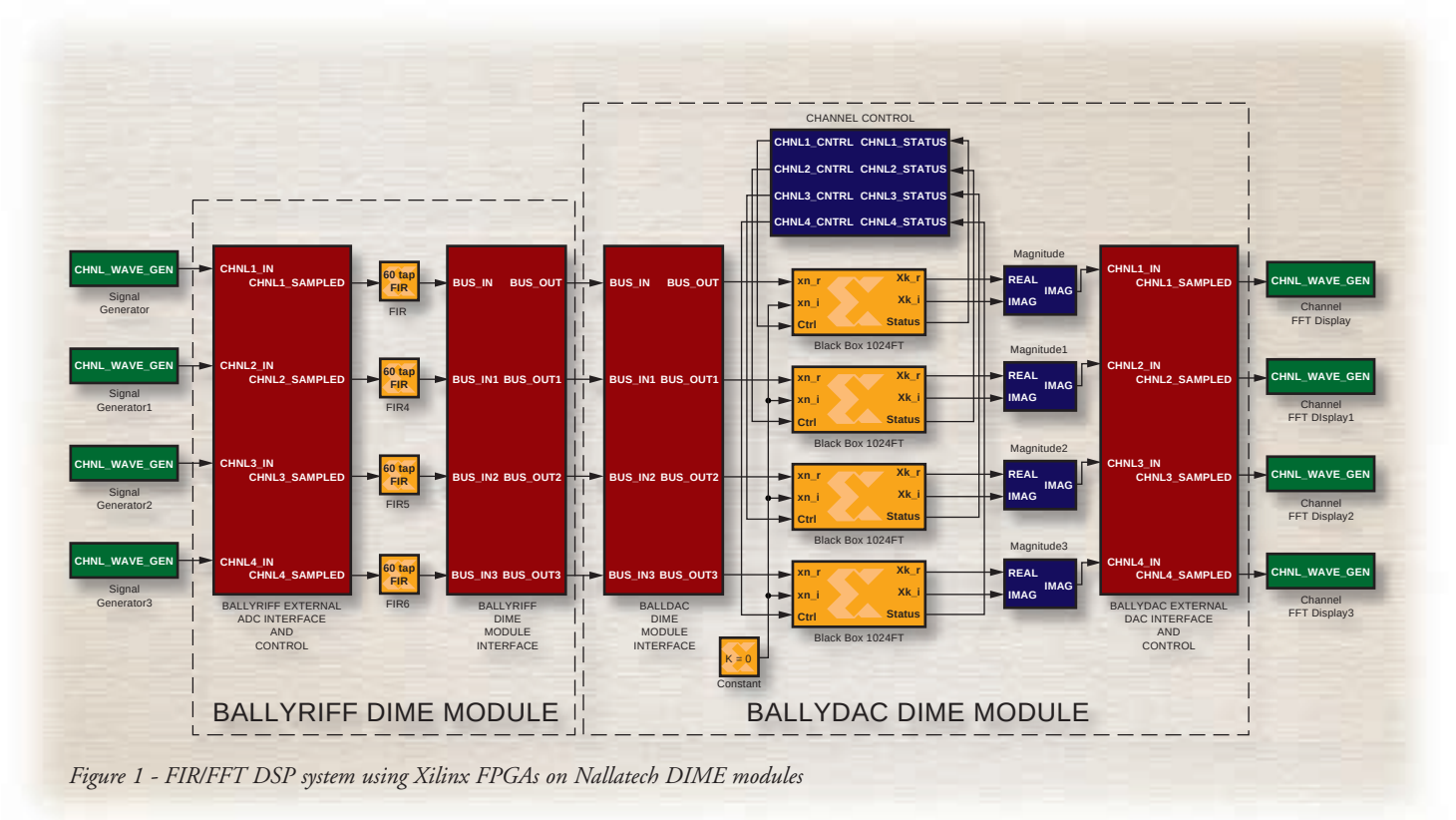

Figure 1 - FIR/FFT DSP system using Xilinx FPGAs on Nallatech DIME modules

As shown in Figure 2 (block diagram) and Figure 3 (actual module), the Ballyriff provides four 12-bit ADC (Analog to Digital Converter) channels, 100 MSPS (Mega Samples Per Second) conversion rate, 128 MB SDRAM for data storage, and can be

Figure 2 - Ballyriff block diagram

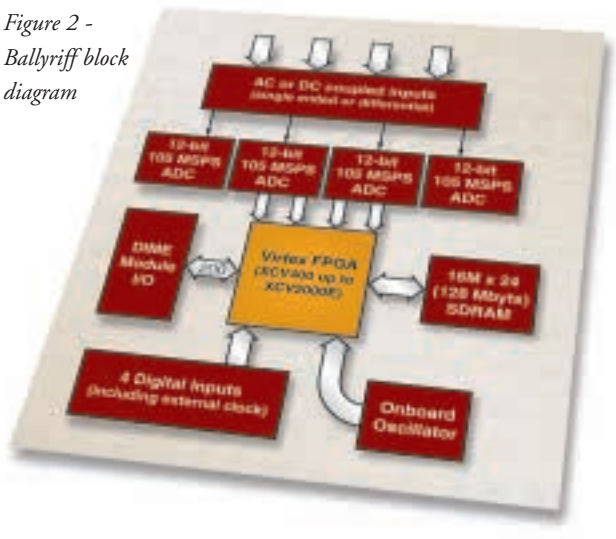

Figure 3 - Ballyriff 4-Channel 100 MSPS 12-bit ADC DIME module

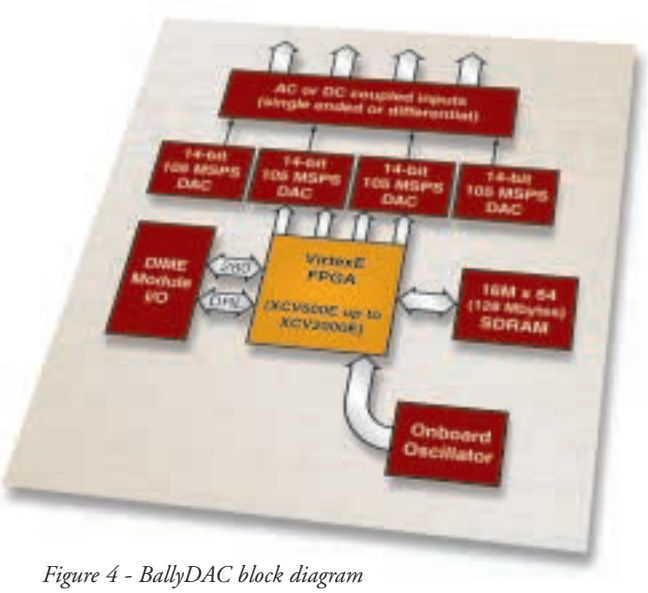

Figure 4 - BallyDAC block diagram

Figure 5 - BallyDAC 4-Channel 150 MSPS 14-bit DAC DIME module

fitted with up to a Virtex™ XCV2000E device (a XCV1000 FPGA is shown here). The Virtex-E FPGA can handle the 600 MB/S (MegaBytes per Second) of I/O bandwidth required to process the data from the ADCs. A 60-tap FIR filter is implemented for each input channel (Figure 1) to provide pre-filtering and noise reduction in the application. The processed data is passed to the adjacent BallyDAC module over the high-speed bus structures available on the Ballynuey2 motherboard.

The BallyDAC DIME module, shown in Figure 4 (block diagram) and Figure 5 (actual module), complements the specifications of the Ballyriff and provides four 14-bit DACs (Digital to Analog Converters), a 150 MSPS conversion rate, 128 MB of SDRAM for storage, and can be fitted with up to a Virtex XCV2000E FPGA to provide the required I/O and processing bandwidth for the DACs. (Figure 5 shows a Virtex XCV1000E device.) The Virtex-E FPGA is configured with a design that carries out a 1,024-point FFT and magnitude calculation, for simple frequency spectrum analysis, on each of the four channels of the captured data that is passed from the Ballyriff DIME module. The resulting magnitude output from the BallyDAC can then be used for further processing or subsequently displayed in real time.

The FFTs are configured in a triple-memory space configuration, and the four channels make full use of the 96 BlockRAM™ available in the XCV1000E device. This highlights just some of the key architectural features of today's FPGAs that prove their suitability for high speed DSP applications.

The DSP Design Challenge

The example system in Figure 1 can be constructed from standard DSP cores from Xilinx. Although these cores can be combined through additional levels of VHDL (Very High Speed Integrated Circuit ((VHSIC)) Hardware Description Language), newer tools, such as the Xilinx System Generator™ for The MathWorks' Simulink™ program, allow designs to be created by DSP engineers without extensive VHDL knowledge.

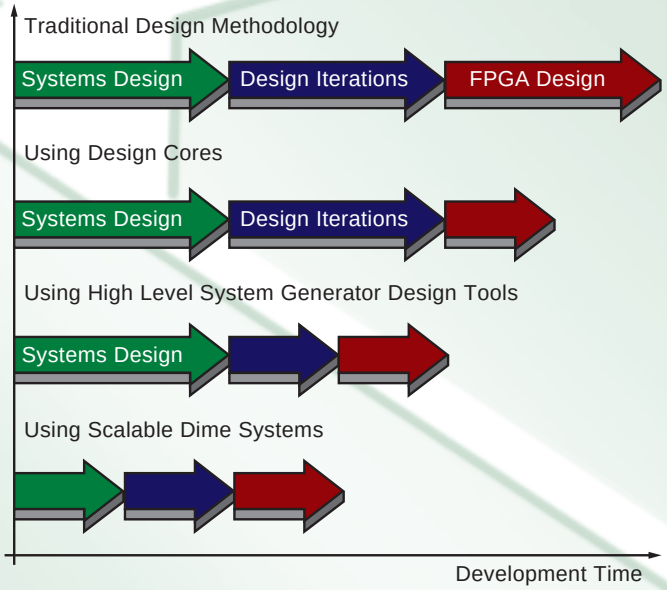

Figure 6 - Development Time

Although FPGAs support the increasing performance requirements, growing complexity, and shorter developments time of today's DSP design challenges, there is still a clear need for a suitable hardware platform to cope with the required external devices and interfaces – and the possibility of partitioning the platform for a multiple FPGA solution. DIME modules from Nallatech provide such a hardware platform. The Ballyriff and BallyDAC boards are just two examples of DIME modules that are particularly suitable for high performance DSP applications. The scalable platform architecture of DIME modules further reduces the development time of systems as illustrated in Figure 6.

Conclusion

Today, system designers require suitable tools, development platforms, and hardware to efficiently create complex high performance DSP systems. Systems that can provide the flexibility of high speed DAC and DSP functionality with the advantages of FPGA resources and a reduced development time are ideal for DSP designers. The advent of tools, such as System Generator from Xilinx and The MathWorks, will ease the development of these DSP systems, aiding the migration of DSP designers to FPGA-based platforms in a familiar environment.

For the latest information on the new Ballynuey3 DIME motherboard and how it uses Virtex-II devices to support encryption and IP protection, visit www.nallatech.com.

FUSE—Field Upgradeable Systems Environment

Nallatech Ltd. offers a "circulation system" to link FPGA platforms with board platforms.

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Xilinx's "Platform FPGA" initiative provides a visionary way forward for the development of a new generation of embedded systems. The Virtex-II™ family of FPGAs are at the heart of the initiative with many new and flexible features from an extensive range of hard and soft intellectual property. Nallatech – a Xilinx XPERTS Partner – has consolidated its board level systems expertise and is complementing the Xilinx effort with the Nallatech systems framework called FUSE™. This "Field Upgradeable Systems Environment" framework provides the fusion between silicon systems and hardware systems, allowing accelerated time to market and in-field support.

The FUSE Design Environment

The FUSE system was initially devised in 1998 as the first system framework to provide greater support to designers who require a distributed FPGA platform. Combined with a highly scalable board platform, the FUSE framework allows the rapid creation of new end products.

As illustrated in Figure 1, the FUSE system has evolved out of the proven framework used by the award-winning DIME (Dsp and Imaging Module for Enhanced fpgas) platforms. (For more information on DIME technology, see "Build Scalable DSP Systems with Nallatech DIME Modules" in this issue of *Xcell Journal*.) DIME-based platforms offer very flexible and scalable modular systems for FPGA-based product development. The goal of the FUSE framework is to provide product systems engineers with the following key benefits:

- **Intelligent hardware** – for Plug and Play
- **Harness latest FPGA developments** – to support Virtex-II family of FPGAs
- **Multiple platform support** – for Windows, Linux, etc.
- **Scalable systems** – to support high end applications
- **Flexibility** – to accelerate time to market
- **High performance and bandwidth** – for high speed communications
- **Field upgradeablity** – to streamline product support
- **Proven technology** – for risk reduction.

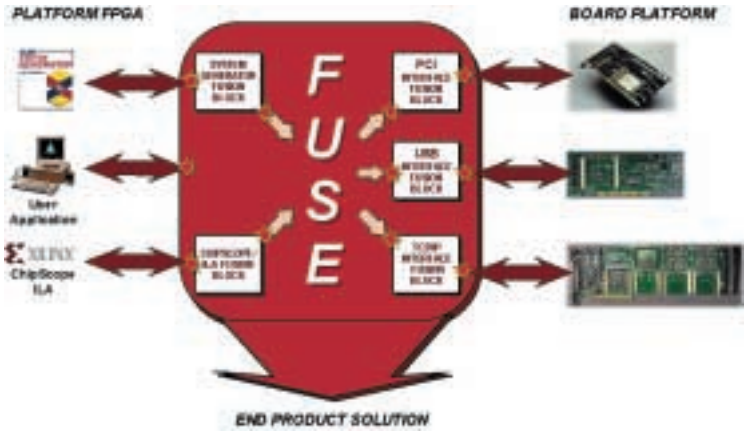

Figure 1 - FUSE: the fusion of the FPGA platform and the board platform

Systems Silicon and Systems Hardware Fusion

The FUSE framework is the circulation system for linking the features currently available for the FPGA platform to those available on a board platform. The FUSE system allows for the integration of features and standards from the board platform, such as DIME modules, with many of the high level design tools such as the Xilinx ChipScope ILA (Integrated Logic Analysis) debugging tool and System Generator software. The FUSE framework offers the capability to easily control and configure distributed FPGA systems, whether they are tightly coupled, such as on a PCI board, or loosely coupled over the Internet. This flexibility, along with the abstraction of the communications channel and control, enables systems engineers to kick start product development and to provide added value.

The creation of this systems environment enables the use and control of intelligent hardware such as Plug and Play detection of attached DIME modules. System hardware, based on the DIME standard, gives the ability to rapidly create ideal physical hardware platforms for many requirements. This is accomplished by harnessing the arsenal of DIME modules that provide a variety of real world interfaces, such as high end ADCs (Analog to Digital Converters), DACs (Digital to