




















Xilinx Application Notes

# Application Notes

◆ [Summaries](#)

Title	Size	Summary	Family	Design
 <a href="#">Loadable Binary Counters</a>	40 KB	<a href="#">XAPP004</a>	XC3000	<a href="#">VIEW/Log/OrCAD</a>
 <a href="#">Register Based FIFO</a>	60 KB	<a href="#">XAPP005</a>	XC3000	<a href="#">VIEW/Log/OrCAD</a>
 <a href="#">Boundary Scan Emulator for XC3000</a>	80 KB	<a href="#">XAPP007</a>	XC3000	<a href="#">VIEW/Log/OrCAD</a>
 <a href="#">Complex Digital Waveform Generator</a>	10 KB	<a href="#">XAPP008</a>	FPGAs	
 <a href="#">Harmonic Frequency Synthesizer and FSK Modulator</a>	20 KB	<a href="#">XAPP009</a>	FPGAs	<a href="#">VIEW/Log/OrCAD</a>
 <a href="#">Bus Structured Serial Input/Output Device</a>	20 KB	<a href="#">XAPP010</a>	XC4000	
 <a href="#">LCA Speed Estimation: Asking the Right Question</a>	10 KB	<a href="#">XAPP011</a>	FPGAs	
 <a href="#">Quadrature Phase Detector</a>	20 KB	<a href="#">XAPP012</a>	XC3000	
 <a href="#">Using the Dedicated Carry Logic in XC4000E</a>	100 KB	<a href="#">XAPP013</a>	XC4000	
 <a href="#">Ultra-Fast Synchronous Counters</a>	40 KB	<a href="#">XAPP014</a>	FPGAs	<a href="#">VIEW/Log/OrCAD</a>
 <a href="#">Using the XC4000 Readback Capability</a>	60 KB	<a href="#">XAPP015</a>	XC4000	
 <a href="#">Boundary Scan in XC4000/XC5200 Device v3.0 (11/99)</a>	100 KB	<a href="#">XAPP017</a>	XC4000 XC5200	
 <a href="#">Estimating the Performance of XC4000E Adders and Counters</a>	40 KB	<a href="#">XAPP018</a>	XC4000	
 <a href="#">Adders, Subtracters and Accumulators in XC3000</a>	60 KB	<a href="#">XAPP022</a>	XC3000	<a href="#">VIEW/Log/OrCAD</a>
 <a href="#">Accelerating Loadable Counters in XC4000</a>	30 KB	<a href="#">XAPP023</a>	XC4000	<a href="#">VIEW/Log/OrCAD</a>
 <a href="#">XC3000 Series Technical Information</a>	110 KB	<a href="#">XAPP024</a>	XC3000	
 <a href="#">Multiplexers and Barrel Shifters in XC3000 Series</a>	40 KB	<a href="#">XAPP026</a>	XC3000	<a href="#">VIEW/Log/OrCAD</a>
 <a href="#">Implementing State Machines in FPGA Devices</a>	30 KB	<a href="#">XAPP027</a>	FPGAs	
 <a href="#">Frequency/Phase Comparator for Phase Locked Loops</a>	40 KB	<a href="#">XAPP028</a>	FPGAs	<a href="#">VIEW/Log/OrCAD</a>
 <a href="#">Serial Code Conversion between BCD and Binary</a>	20 KB	<a href="#">XAPP029</a>	XC3000	<a href="#">VIEW/Log/OrCAD</a>

## DataSource CD-ROM Q4-01: Application Notes (continued)

Title	Size	Summary	Family	Design
 <a href="#">Megabit FIFO in Two Chips: One LCA Device and One DRAM</a>	20 KB	<a href="#">XAPP030</a>	XC3000	
 <a href="#">Improving XC4000 Design Performance</a>	160 KB	<a href="#">XAPP043</a>	XC4000	
 <a href="#">XC4000 Series Technical Information</a>	30 KB	<a href="#">XAPP045</a>	XC4000	
 <a href="#">Synchronous and Asynchronous FIFO Designs</a>	120 KB	<a href="#">XAPP051</a>	XC4000	
 <a href="#">Efficient Shift Registers, LFSR Counters, and Long Pseudo-Random Sequence Generators</a>	70 KB	<a href="#">XAPP052</a>	XC4000	
 <a href="#">Implementing FIFOs in XC4000 Series RAM</a>	220 KB	<a href="#">XAPP053</a>	XC4000	<a href="#">VIEW/og</a>
 <a href="#">Constant Coefficient Multipliers for the XC4000E</a>	110 KB	<a href="#">XAPP054</a>	XC4000	
 <a href="#">Block Adaptive Filter</a>	120 KB	<a href="#">XAPP055</a>	XC4000	
 <a href="#">System Design with New XC4000X I/O Features</a>	70 KB	<a href="#">XAPP056</a>	XC4000	
 <a href="#">Using SelectRAM Memory in XC4000 Series FPGAs</a>	140 KB	<a href="#">XAPP057</a>	XC4000	
 <a href="#">Xilinx In-System Programming Using an Embedded Microcontroller v3.0 (01/15/01)</a>	590 KB	<a href="#">XAPP058</a>	All	<a href="#">PC Solaris HP</a>
 <a href="#">Gate Count Capacity Metrics for FPGAs</a>	80 KB	<a href="#">XAPP059</a>	FPGAs	
 <a href="#">Design Migration from XC4000 to XC5200</a>	120 KB	<a href="#">XAPP060</a>	XC4000 XC5200	
 <a href="#">Design Migration from XC2000/XC3000 to XC5200</a>	70 KB	<a href="#">XAPP061</a>	XC2000 XC3000 XC5200	
 <a href="#">Design Migration from XC4000 to XC4000E</a>	60 KB	<a href="#">XAPP062</a>	XC4000	
 <a href="#">XC4000 Series Edge-Triggered and Dual-Port RAM Capability</a>	50 KB	<a href="#">XAPP065</a>	XC4000	
 <a href="#">Using Serial Vector Format Files to Program XC9500 Devices In-System on Automatic Test Equipment and Third Party Tools</a>	40 KB	<a href="#">XAPP067</a>	XC9500	
 <a href="#">In-System Programming Times</a>	10 KB	<a href="#">XAPP068</a>	XC9500	
 <a href="#">Using the XC9500 JTAG Boundary Scan Interface</a>	120 KB	<a href="#">XAPP069</a>	XC9500	
<b>Title</b>	<b>Size</b>	<b>Summary</b>	<b>Family</b>	<b>Design</b>
 <a href="#">Using In-System Programmability in Boundary Scan Systems</a>	40 KB	<a href="#">XAPP070</a>	XC9500	
 <a href="#">Using the XC9500 Timing Model</a>	60 KB	<a href="#">XAPP071</a>	XC9500	
 <a href="#">Designing with XC9500 CPLDs</a>	100 KB	<a href="#">XAPP073</a>	XC9500	
 <a href="#">Pin Preassigning with XC9500 CPLDs</a>	50 KB	<a href="#">XAPP074</a>	XC9500	
 <a href="#">Embedded Instrumentation Using XC9500 CPLDs</a>	50 KB	<a href="#">XAPP076</a>	XC9500	
 <a href="#">XC9536 ISP Demo Board</a>	50 KB	<a href="#">XAPP078</a>	XC9500	<a href="#">ABEL VHDL</a>
 <a href="#">Configuring Xilinx FPGAs Using an XC9500 CPLD and Parallel PROM v1.1 (07/27/00)</a>	100 KB	<a href="#">XAPP079</a>	XC9500	
 <a href="#">Supply Voltage Migration, 5 V to 3.3 V</a>	30 KB	<a href="#">XAPP080</a>	XC4000	
 <a href="#">I/O Characteristics of the 'XL FPGAs</a>	30 KB	<a href="#">XAPP088</a>	Spartan XC4000	
 <a href="#">FPGA Configuration Guidelines</a>	60 KB	<a href="#">XAPP090</a>	FPGAs	
 <a href="#">Configuring Mixed FPGA Daisy Chains</a>	20 KB	<a href="#">XAPP091</a>	FPGAs	
 <a href="#">Configuration Issues: Power-up, Volatility, Security, Battery Back-up</a>	30 KB	<a href="#">XAPP092</a>	FPGAs	
 <a href="#">Dynamic Reconfiguration</a>	20 KB	<a href="#">XAPP093</a>	FPGAs	
 <a href="#">Metastable Recovery</a>	20 KB	<a href="#">XAPP094</a>	FPGAs	

## DataSource CD-ROM Q4-01: Application Notes (continued)

 <a href="#">Set-up and Hold Times</a>	10 KB	<a href="#">XAPP095</a>	FPGAs	
 <a href="#">Overshoot and Undershoot</a>	10 KB	<a href="#">XAPP096</a>	FPGAs	
 <a href="#">Xilinx FPGAs: A Technical Overview for the First Time User</a>	20 KB	<a href="#">XAPP097</a>	FPGAs	
 <a href="#">The Low-Cost, Efficient Serial Configuration of Spartan FPGAs</a>	100 KB	<a href="#">XAPP098</a>	Spartan	
 <a href="#">Choosing a Xilinx Product Family</a>	30 KB	<a href="#">XAPP100</a>	All	
 <a href="#">XC9500 Remote Field Upgrade</a>	80 KB	<a href="#">XAPP102</a>	XC9500	<a href="#">PC</a> <a href="#">UNIX</a>
 <a href="#">The Tagalyzer - A JTAG Boundary Scan Debug Tool</a>	130 KB	<a href="#">XAPP103</a>	XC9500	
 <a href="#">A Quick JTAG ISP Checklist</a>	20 KB	<a href="#">XAPP104</a>	XC9500	
 <a href="#">A CPLD VHDL Introduction</a> v2.0 (08/30/01) <b>UPDATE!</b>	333 KB	<a href="#">XAPP105</a>	XC9500	
 <a href="#">Synopsys/Xilinx High Density Design Methodology Using FPGA Compiler</a>	240 KB	<a href="#">XAPP107</a>	XC4000X	
 <a href="#">Chip-Level HDL Simulation Using the Xilinx Alliance Series</a> v2.0 (05/22/00)	165 KB	<a href="#">XAPP108</a>	FPGAs	
 <a href="#">Hints, Tips and Tricks for Using XABEL with Xilinx M1.5 Design and Implementation Tools</a>	80 KB	<a href="#">XAPP109</a>	All	
 <a href="#">XC9500 CPLD Power Sequencing</a>	30 KB	<a href="#">XAPP110</a>	XC9500	
 <a href="#">Using the XC9500XL Timing Model</a> v1.3 (08/20/01) <b>UPDATE!</b>	72 KB	<a href="#">XAPP111</a>	XC9500XL	
 <a href="#">Designing With XC9500XL CPLDs</a>	160 KB	<a href="#">XAPP112</a>	XC9500XL	
 <a href="#">Faster Erase Times for XC95216 and XC95108 Devices on HP 3070 Series Testers</a>	30 KB	<a href="#">XAPP113</a>	XC9500	
 <a href="#">Understanding XC9500XL CPLD Power</a>	90 KB	<a href="#">XAPP114</a>	XC9500XL	
 <a href="#">Planning for High Speed XC9500XL Designs</a>	100 KB	<a href="#">XAPP115</a>	XC9500XL	
 <a href="#">Adapting ASIC Designs for Use with Spartan FPGAs</a>	50 KB	<a href="#">XAPP119</a>	Spartan	
 <a href="#">How Spartan FPGAs -- The Gate Array Solution</a>	87 KB	<a href="#">XAPP120</a>	Spartan	
 <a href="#">The Express Configuration of Spartan-XL FPGAs</a> (v3.0) 4/19/01	141 KB	<a href="#">XAPP122</a>	Spartan-XL	
 <a href="#">Using Three-State Enable Registers in XLA, XV, and Spartan-XL FPGAs</a>	40 KB	<a href="#">XAPP123</a>	XC4000XLA XC4000XV Spartan-XL	<a href="#">PC</a> <a href="#">UNIX</a>
 <a href="#">Using Manual Power Down Mode With Spartan-XL FPGAs</a>	20 KB	<a href="#">XAPP124</a>	Spartan-XL	
 <a href="#">Conserving Power With Auto Power Down Mode in Spartan-XL FPGAs</a>	20 KB	<a href="#">XAPP125</a>	Spartan-XL	
 <a href="#">Data Generation and Configuration for Spartan Series FPGAs</a>	80 KB	<a href="#">XAPP126</a>	Spartan	
<b>Title</b>	<b>Size</b>	<b>Summary</b>	<b>Family</b>	<b>Design</b>
 <a href="#">Using the Virtex Block SelectRAM+ Features</a> v1.4 (12/18/00)	95 KB	<a href="#">XAPP130</a>	Virtex	
 <a href="#">170 MHz FIFOs Using the Virtex Block SelectRAM+ Feature</a> v1.5 (06/06/01)	75 KB	<a href="#">XAPP131</a>	Virtex	<a href="#">PC</a> <a href="#">UNIX</a>
 <a href="#">Using the Virtex Delay-Locked Loop</a> v2.3 (09/20/00)	90 KB	<a href="#">XAPP132</a>	Virtex	
 <a href="#">Using the Virtex Select/O Resource</a> v2.4 (04/17/00)	230 KB	<a href="#">XAPP133</a>	Virtex	
 <a href="#">Virtex Synthesizable High Performance SDRAM Controller</a> v3.1 (02/01/00)	105 KB	<a href="#">XAPP134</a>	Virtex	<a href="#">PC:VHDL</a> <a href="#">PC:Verilog</a> <a href="#">UNIX:VHDL</a> <a href="#">UNIX:Verilo</a>

## DataSource CD-ROM Q4-01: Application Notes (continued)

 <a href="#">Virtex I/V Curves for Various Output Options</a>	20 KB	<a href="#">XAPP135</a>	Virtex	
 <a href="#">Synthesizable 143 MHz ZBT SRAMInterface v2.0 (01/00)</a>	90 KB	<a href="#">XAPP136</a>	Virtex	<a href="#">PC</a> <a href="#">UNIX</a>
 <a href="#">Configuring Virtex FPGAs from Parallel EPROMs with a CPLD</a>	90 KB	<a href="#">XAPP137</a>	Virtex XC9500	<a href="#">PC</a>
 <a href="#">Virtex Configuration and Readback v2.4 (07/25/01)</a>	533 KB	<a href="#">XAPP138</a>	Virtex	
 <a href="#">Configuration and Readback of Virtex FPGAs Using (JTAG) Boundary-Scan v1.2 (2/00)</a>	88 KB	<a href="#">XAPP139</a>	Virtex/-E	
 <a href="#">In-System Programming Times for XC9500XL</a>	10 KB	<a href="#">XAPP141</a>	XC9500XL	
 <a href="#">Designing CPLD Multi-voltage Systems v1.3 (03/00)</a>	65 KB	<a href="#">XAPP144</a>	CPLD	
 <a href="#">Designing an Eight Channel Digital Volt Meter with the Insight Springboard Kit (v1.0) 4/30/01</a>	58 KB	<a href="#">XAPP146</a>	CoolRunner CPLD	
 <a href="#">Low Power Handspring Springboard Module Design with CoolRunner CPLDs (v1.0) 1/25/01</a>	56 KB	<a href="#">XAPP147</a>	CoolRunner CPLD	
 <a href="#">I/V Curves for Various Device Families</a>	20 KB	<a href="#">XAPP150</a>	All	
 <a href="#">Virtex Series Configuration Architecture User Guide v1.4 (08/03/00)</a>	245 KB	<a href="#">XAPP151</a>	Virtex	
 <a href="#">Virtex Power Estimator User Guide v1.1 (2/00)</a>	90 KB	<a href="#">XAPP152</a>	Virtex	<a href="#">worksheet</a>
 <a href="#">Status and Control Semaphore Registers Using Partial Reconfiguration</a>	180 KB	<a href="#">XAPP153</a>	Virtex	<a href="#">PC</a>
 <a href="#">Virtex Synthesizable Delta-Sigma DAC</a>	60 KB	<a href="#">XAPP154</a>	Virtex	
 <a href="#">Virtex Analog to Digital Converter</a>	50 KB	<a href="#">XAPP155</a>	Virtex	
 <a href="#">Board Routability Guidelines with Xilinx Fine-Pitch BGA Packages v1.0 (07/26/00)</a>	1,800 KB	<a href="#">XAPP157</a>	Virtex	
 <a href="#">Powering Virtex FPGAs v1.4 (02/06/01)</a>	70 KB	<a href="#">XAPP158</a>	Virtex	
 <a href="#">XC1700 and XC18V00 Design Migration Considerations</a>	60 KB	<a href="#">XAPP161</a>	XC1700E/L, XC1800	
 <a href="#">Using Xilinx and Synplify for Incremental Designing (ECO)</a>	40 KB	<a href="#">XAPP164</a>	FPGA	<a href="#">PC</a> <a href="#">UNIX</a>
 <a href="#">Using Xilinx and Exemplar for Incremental Designing (ECO)</a>	70 KB	<a href="#">XAPP165</a>	FPGA	<a href="#">PC</a> <a href="#">UNIX</a>
 <a href="#">TAU/BLAST Support in 2.1i</a>	20 KB	<a href="#">XAPP166</a>	FPGA	
 <a href="#">Getting Started With the MultiLINX Cable v1.2 (04/20/00)</a>	180 KB	<a href="#">XAPP168</a>	FPGA	
 <a href="#">MP3 NG: A Next Generation Consumer Platform v1.0 (01/00)</a>	360 KB	<a href="#">XAPP169</a>	Spartan-II	
<a href="#">Implementing an ISDN PCMCIA Modem Using Spartan Devices v1.0 (7/99)</a>		<a href="#">XAPP170</a>	Spartan	
<a href="#">Implementing an ADSL to USB Interface Using Spartan Devices v1.0 (3/99)</a>		<a href="#">XAPP171</a>	Spartan	
<a href="#">The Design of a Video Capture Board Using the Spartan Series v1.0 (3/99)</a>		<a href="#">XAPP172</a>	Spartan	
 <a href="#">Using Block SelectRAM+ Memory in Spartan-II FPGAs v1.1 (12/11/00)</a>	100 KB	<a href="#">XAPP173</a>	Spartan-II	
 <a href="#">Using Delay-Locked Loops in Spartan-II FPGAs v1.0 (01/00)</a>	120 KB	<a href="#">XAPP174</a>	Spartan-II	<a href="#">PC</a> <a href="#">UNIX</a>
 <a href="#">High Speed FIFOs In Spartan-II FPGAs v1.0 (01/00)</a>	50 KB	<a href="#">XAPP175</a>	Spartan-II	<a href="#">PC</a> <a href="#">UNIX</a>
 <a href="#">Spartan-II FPGA Family Configuration and Readback v1.0 (01/00)</a>	400 KB	<a href="#">XAPP176</a>	Spartan-II	

## DataSource CD-ROM Q4-01: Application Notes (continued)

 <a href="#">Spartan-Family I/V Curves for Various Output Options</a> v1.0 (01/00)	30 KB	<a href="#">XAPP177</a>	Spartan-II	
 <a href="#">Configuring Spartan-II FPGAs from Parallel EPROMs</a> v1.0 (01/00)	100 KB	<a href="#">XAPP178</a>	Spartan-II	<a href="#">PC</a>
 <a href="#">Using Select/O Interfaces in Spartan-II FPGAs</a> v1.0 (01/00)	300 KB	<a href="#">XAPP179</a>	Spartan-II	
 <a href="#">SEU Mitigation Design Techniques for the XQR4000XL</a> v1.0 (03/15/00)	105 KB	<a href="#">XAPP181</a>	FPGA	
 <a href="#">Configuration and Readback of Spartan-II FPGAs Using Boundary Scan</a> (v2.0) 4/19/01	166 KB	<a href="#">XAPP188</a>	Spartan-II	
 <a href="#">Powering Xilinx Spartan-II FPGAs</a> v1.1 (07/20/01)	78 KB	<a href="#">XAPP189</a>	Spartan-II	
 <a href="#">Interfacing a Virtex-E Device to a MIPS Processor</a> v1.0 (12/15/00)	100 KB	<a href="#">XAPP192</a>	Virtex	
 <a href="#">Interfacing a Virtex-E Device to a Pentium Processor</a> v1.0 (12/15/00)	70 KB	<a href="#">XAPP196</a>	Virtex	
 <a href="#">Synthesizable FPGA Interface for Retrieving ROM Number from 1-Wire Devices</a> v1.0 (05/08/01)	165 KB	<a href="#">XAPP198</a>	Virtex, Spartan-II	
 <a href="#">Writing Efficient Testbenches</a> v1.0 (06/18/01)	279 KB	<a href="#">XAPP199</a>	Test Benches	<a href="#">PC</a> <a href="#">UNIX</a>
 <a href="#">Virtex Synthesizable 1.6 Gbytes/s DDR SDRAM Controller</a> v2.3 (03/21/00)	105 KB	<a href="#">XAPP200</a>	Virtex	<a href="#">PC</a>
 <a href="#">An Overview of Multiple CAM Designs in Virtex Devices</a>	40 KB	<a href="#">XAPP201</a>	Virtex	
 <a href="#">Content Addressable Memory (CAM) in ATM Applications</a> v1.2 (01/06/01)	140 KB	<a href="#">XAPP202</a>	Virtex, Virtex-II	<a href="#">PC</a>
 <a href="#">Designing Flexible, Fast CAMs with Virtex Slices</a>	100 KB	<a href="#">XAPP203</a>	Virtex	<a href="#">PC</a> <a href="#">UNIX</a>
 <a href="#">Using Block RAM for High-Performance Read/Write CAMs</a> v1.2 (05/02/00)	100 KB	<a href="#">XAPP204</a>	Virtex	
 <a href="#">Data-Width Conversion FIFOs Using the Virtex Block SelectRAM Memory</a> v1.3 (08/10/00)	50 KB	<a href="#">XAPP205</a>	Virtex	
 <a href="#">An Inverse Discrete Cosine Transform (IDCT) Implementation in Virtex Devices for MPEG Video Applications</a> v1.1 (01/00)	40 KB	<a href="#">XAPP208</a>	Virtex	<a href="#">design</a>
 <a href="#">IEEE 802.3 Cyclic Redundancy Check</a> v1.0 (03/23/01)	120 KB	<a href="#">XAPP209</a>	Virtex-II	
 <a href="#">Linear Feedback Shift Registers in Virtex Devices</a> v1.2 (01/09/01)	85 KB	<a href="#">XAPP210</a>	Virtex, Virtex-II	
 <a href="#">PN Generators Using the SRL Macro</a> v1.1 (01/09/01)	120 KB	<a href="#">XAPP211</a>	Virtex, Virtex-II, Spartan-II	
 <a href="#">CDMA Matched Filter Implementation in Virtex Devices</a> v1.1 (01/10/01)	170 KB	<a href="#">XAPP212</a>	Virtex, Virtex-II, Spartan-II	
 <a href="#">8-Bit Microcontroller for Virtex Devices</a> v1.0 (09/25/00)	380 KB	<a href="#">XAPP213</a>	Virtex, Spartan-II	
 <a href="#">Design Tips for HDL Implementation of Arithmetic Functions</a> v1.0 (06/28/00)	78KB	<a href="#">XAPP215</a>	Virtex	
 <a href="#">Correcting Single-Event Upsets Through Virtex Partial Configuration</a> v1.0 (06/01/00)	110 KB	<a href="#">XAPP216</a>	Virtex	
 <a href="#">Gold Code Generators in Virtex Devices</a> v1.1 (01/10/01)	125 KB	<a href="#">XAPP217</a>	Virtex, Virtex-II, Spartan-II	
 <a href="#">Transposed Form FIR Filters</a> v1.1 (01/10/01)	150 KB	<a href="#">XAPP219</a>	Virtex, Virtex-II	
 <a href="#">LFSRs as Functional Blocks in Wireless</a>	135 KB	<a href="#">XAPP220</a>	Virtex, Virtex-II, Spartan-II	

## DataSource CD-ROM Q4-01: Application Notes (continued)


 <a href="#">200 MHz UART with Internal 16-Byte Buffer</a> v1.1 (07/10/01)	150 KB	<a href="#">XAPP223</a>	Virtex, Virtex-II, Spartan-II
 <a href="#">Data Recovery in Virtex and Virtex-II Devices</a> v1.1 (01/10/01)	60 KB	<a href="#">XAPP224</a>	Virtex, Virtex-II
 <a href="#">Data to Clock Phase Alignment</a> v1.0 (09/18/01) <b>NEW!</b>	48 KB	<a href="#">XAPP225</a>	Virtex Series
 <a href="#">The LVDS I/O Standard</a>	70 KB	<a href="#">XAPP230</a>	Virtex-E
 <a href="#">Multi-Drop LVDS with Virtex-E FPGAs</a>	85 KB	<a href="#">XAPP231</a>	Virtex-E
 <a href="#">Virtex-E LVDS Drivers &amp; Receivers: Interface Guidelines</a> v1.0 (11/99)	85 KB	<a href="#">XAPP232</a>	Virtex-E
 <a href="#">Multi-Channel 622 Mb/s LVDS Data Transfer for Virtex-E Devices</a> v1.2 (01/06/01)	260 KB	<a href="#">XAPP233</a>	Virtex-E
 <a href="#">Virtex SelectLink Communications Channel</a> v1.0 (12/99)	25 KB	<a href="#">XAPP234</a>	Virtex-E
 <a href="#">Virtex Package Compatibility Guide</a> v1.3 (06/20/00)	40 KB	<a href="#">XAPP235</a>	Virtex
 <a href="#">LVDS System Data Framing</a> v1.0 (12/18/00)	80 KB	<a href="#">XAPP238</a>	Virtex-E
 <a href="#">High-Speed Buffered Crossbar Switch Design Using Virtex-EM Devices</a> v1.0 (03/14/00)	80 KB	<a href="#">XAPP240</a>	Virtex-EM
 <a href="#">Virtex-EM FIR Filter for Video Applications</a> v1.0 (03/14/00)	60 KB	<a href="#">XAPP241</a>	Virtex-EM
 <a href="#">Interfacing to Lara Networks Search Engine Using Virtex Devices</a> v1.0 (06/08/00)	80 KB	<a href="#">XAPP242</a>	Virtex-EM
 <a href="#">Eight Channel, One Clock, One Frame LVDS Transmitter/Receiver</a> v1.0 (03/02/01)	148 KB	<a href="#">XAPP245</a>	Virtex-E
 <a href="#">PowerPC 60X Bus Interface to a Virtex-E Device</a> v1.0 (12/15/00)	165 KB	<a href="#">XAPP246</a>	Virtex-E <a href="#">PC</a>
 <a href="#">Hot-Swapping Virtex-II Devices</a> v1.1 (08/15/01) <b>UPDATE!</b>	65 KB	<a href="#">XAPP251</a>	Virtex-II
 <a href="#">Synthesizable 266 MBits/s DDR SDRAM Controller</a> v1.0 (01/12/01)	155 KB	<a href="#">XAPP253</a>	Virtex-II
 <a href="#">The Virtex-II SiberBridge</a> v1.0 (01/12/01)	120 KB	<a href="#">XAPP254</a>	Virtex-II
 <a href="#">FIFOs Using Virtex-II Shift Registers</a> v1.0 (01/15/01)	50 KB	<a href="#">XAPP256</a>	Virtex-II
 <a href="#">FIFOs Using Virtex-II Block RAM</a> v1.2 (06/05/01)	60 KB	<a href="#">XAPP258</a>	Virtex-II
 <a href="#">Data-Width Conversion FIFOs Using the Virtex-II Block RAM Memory</a> v1.0 (01/10/01)	80 KB	<a href="#">XAPP261</a>	Virtex-II
 <a href="#">Quad DataRate (QDR) SRAM Interface for Virtex-II Devices</a> v1.0 (01/15/01)	80 KB	<a href="#">XAPP262</a>	Virtex-II
 <a href="#">Parity Generation and Validation in Virtex-II Devices</a> v1.0 (01/15/01)	45 KB	<a href="#">XAPP267</a>	Virtex-II
 <a href="#">High-Speed DES and Triple DES Encryptor/Decryptor</a> v1.0 (10/01/01) <b>NEW!</b>	151 KB	<a href="#">XAPP270</a>	Virtex-II
 <a href="#">Color Space Converter</a> v1.0 (07/11/01)	110 KB	<a href="#">XAPP283</a>	Virtex-II <a href="#">PC</a>
 <a href="#">3 x 3 Matrix Multiplier for 3D Graphics and Video</a> v1.0 (07/11/01)&	75 KB	<a href="#">XAPP284</a>	Virtex-II <a href="#">PC</a>
 <a href="#">Common Switch Interface CSIX-L1 Reference Design</a> v1.0 (08/10/01) <b>NEW!</b>	88 KB	<a href="#">XAPP289</a>	Virtex-II



## DataSource CD-ROM Q4-01: Application Notes (continued)

Title	Size	Summary	Family	Desig
 <a href="#">In-System Programming (ISP)</a>	80 KB	<a href="#">XAPP300</a>	CoolRunner	
 <a href="#">Power Up Reset Characteristics of CoolRunner CPLDs</a> v1.1 (12/00)	30 KB	<a href="#">XAPP310</a>	CoolRunner	
 <a href="#">Five Volt Tolerance and PCI</a> v1.1 (2/00)	70 KB	<a href="#">XAPP311</a>	CoolRunner	
 <a href="#">Differences In ABEL and PHDL</a> v1.0 11/99)	60 KB	<a href="#">XAPP312</a>	CoolRunner	
 <a href="#">Design of an MP3 Portable Player Using a CoolRunner CPLD</a> v1.1 (12/99) >	450 KB	<a href="#">XAPP328</a>	CoolRunner	
 <a href="#">Understanding True CMOS Outputs</a> v1.0 (02/00)	90 KB	<a href="#">XAPP329</a>	CoolRunner	
 <a href="#">Pin Locking in CoolRunner XPLA3 CPLDs</a> v1.0 (01/07/00)	80 KB	<a href="#">XAPP332</a>	CoolRunner	
 <a href="#">CoolRunner XPLA3 I<sup>2</sup>C Bus Controller Implementation</a> v1.4 (07/21/00)	170 KB	<a href="#">XAPP333</a>	CoolRunner	
 <a href="#">Utilizing XPLA3 Universal Control Terms</a> v1.0 (01/19/00)	65 KB	<a href="#">XAPP334</a>	CoolRunner	
 <a href="#">Macrocell Configurations in CoolRunner XPLA3 CPLDs</a> v1.0 (04/17/00)	100 KB	<a href="#">XAPP335</a>	CoolRunner	
 <a href="#">Design of a 16b/20b Encoder/Decoder Using a CoolRunner CPLD</a> v1.0 (07/15/00)	280 KB	<a href="#">XAPP336</a>	CoolRunner	
 <a href="#">Using Xilinx WebPACK and ModelTech ModelSim Xilinx Edition (MXE)</a> v1.0 (04/12/00)	2,360 KB	<a href="#">XAPP338</a>	CoolRunner	
 <a href="#">Manchester Encoder-Decoder for Xilinx CPLDs</a> v1.1 (04/17/00)	60 KB	<a href="#">XAPP339</a>	CoolRunner	
 <a href="#">UARTs in Xilinx CPLDs</a> v1.2 (11/28/00)	35 KB	<a href="#">XAPP341</a>	CoolRunner	
 <a href="#">XPLA3 I/O Cell Characteristics</a> v1.0 (04/06/01)	58 KB	<a href="#">XAPP342</a>	CoolRunner	
 <a href="#">In-System Programming of XPLA3 Devices</a> v1.0 (08/30/00)	60 KB	<a href="#">XAPP343</a>	CoolRunner	
 <a href="#">IrDA and UART Design in a CoolRunner CPLD</a> v1.0 (08/08/01) <b>NEW!</b>	132 KB	<a href="#">XAPP345</a>	CoolRunner	
 <a href="#">Low Power Tips for CoolRunner Design</a> v1.0 (10/16/00)	285 KB	<a href="#">XAPP346</a>	CoolRunner	
 <a href="#">Decrease Processor Power Consumption Using a CoolRunner CPLD</a> v1.0 (06/01/01)	82 KB	<a href="#">XAPP347</a>	CoolRunner	
 <a href="#">CoolRunner XPLA3 Serial Peripheral Interface Master</a> v1.0 (11/29/00)	215 KB	<a href="#">XAPP348</a>	CoolRunner	
 <a href="#">CoolRunner CPLD 8051 Microcontroller Interface</a> v1.0 (12/07/00)	105 KB	<a href="#">XAPP349</a>	CoolRunner	
 <a href="#">Implementing HDL with WebPACK ECS Schematic Editor</a> v1.0 (12/20/00)	265 KB	<a href="#">XAPP350</a>	CoolRunner	
 <a href="#">The CoolRunner CPLD IRL Demo: An Example of Using the Internet to Configure a CoolRunner CPLD</a> v1.0 (11/07/00)	557 KB	<a href="#">XAPP351</a>	CoolRunner	
 <a href="#">Utilizing a User Constraint File for CoolRunner CPLDs</a> v1.0 (06/20/01)>	121 KB	<a href="#">XAPP352</a>	CoolRunner	
 <a href="#">CoolRunner XPLA3 SMBus Controller Implementation</a> v1.0 (02/14/01)	179 KB	<a href="#">XAPP353</a>	CoolRunner	
 <a href="#">Using Xilinx CPLDs to Interface to a NAND Flash Memory Device</a> v1.0 (08/30/01) <b>NEW!</b>	520 KB	<a href="#">XAPP354</a>	CoolRunner	
 <a href="#">Serial ADC Interface Using a CoolRunner CPLD</a> v1.0 (04/30/01)	320 KB	<a href="#">XAPP355</a>	CoolRunner	
 <a href="#">CoolRunner Visor Springboard LED Test</a> v1.1 (06/25/01)	320 KB	<a href="#">XAPP357</a>	CoolRunner	
 <a href="#">Understanding the Insight Springboard Development Kit</a> v1.0 (04/30/01)	38 KB	<a href="#">XAPP359</a>	CoolRunner	
 <a href="#">Using the XC9500XV Timing Model</a> v1.0 (08/20/01) <b>NEW!</b>	72 KB	<a href="#">XAPP362</a>	XC9500XV CPLD	

## DataSource CD-ROM Q4-01: Application Notes (continued)

Title	Size	Summary	Family	Desig
 <a href="#">Constraining Virtex Design in 2.1i</a> v1.0 (10/01/99)	125 KB	<a href="#">XAPP400</a>	Virtex	
 <a href="#">2.1i FPGA Editor</a> v1.0 (10/13/99)>	60 KB	<a href="#">XAPP401</a>	Virtex	
 <a href="#">2.1i Floorplanner Support for Virtex FPGAs</a> v1.0 (10/13/99)	530 KB	<a href="#">XAPP402</a>	Virtex	
 <a href="#">Using the Version 2.1i Xilinx Design Manager and Flow Engine (DMFE)</a> v1.0 (09/27/99)	170 KB	<a href="#">XAPP403</a>	Virtex	
 <a href="#">Xilinx Alliance 3.1i Modular Design</a> v1.2 (04/20/01)	690 KB	<a href="#">XAPP404</a>	Virtex	
 <a href="#">Cross Probing to Synplicity and Exemplar</a> v2.0 (12/01/00)	325 KB	<a href="#">XAPP406</a>	FPGA	
 <a href="#">Rethinking Your Verification Strategies for Multimillion-Gate FPGAs</a> v1.0 (10/07/00)	140 KB	<a href="#">XAPP408</a>	FPGAs	
 <a href="#">Simulating a Xilinx 3.1i CORE Generator VHDL Design</a> v1.0 (06/18/01)	185 KB	<a href="#">XAPP409</a>	FPGAs	
 <a href="#">Simulating a Xilinx 3.1i CORE Generator Verilog Design</a> v1.0 (06/18/01)	138 KB	<a href="#">XAPP410</a>	FPGAs	
 <a href="#">Architecting Systems for Upgradability with IRL (Internet Reconfigurable Logic)</a> v1.0 (06/29/01)	150 KB	<a href="#">XAPP412</a>	FPGA	
 <a href="#">J Drive: In-System Programming of IEEE Standard 1532 Devices</a> v1.1 (01/17/01)	150 KB	<a href="#">XAPP500</a>	Virtex	
 <a href="#">Configuration Quick Start Guidelines</a> v1.2 (08/02/01) 	360 KB	<a href="#">XAPP501</a>	All	