Quadrature Phase Decoder

XAPP 012.001

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Summary

A simple state machine is used to adapt the output of two photo-cells to control an up/down counter. The state machine provides hysteresis for counting parts correctly, regardless of changes in direction.

Specifications

Maximum Clock Frequency	~150 MHz
Number of CLBs	2

Xilinx Family

XC3000/XC3100

Demonstrates

State-Machine Design

Introduction

A common technique for counting objects is to pass them through a light beam. Problems can arise, however, if a part dithers on the edge of the light beam and is counted more than once, or if the direction of motion changes and a part is recounted rather than uncounted.

These problems may be avoided by using two sensors, as shown in Figure 1. To be counted, an object must first obscure one sensor, then obscure the other, clear the first and finally clear the second. This solves the dither problem as an object must pass entirely through the beam before it can be counted. Sensor signals resulting from the object dithering while entering or leaving the beam will be ignored by the counter.

The direction of motion determines the order in which the sensors are first obscured and then cleared. A state machine recognizes the order and controls an up/down counter to correctly account for parts that pass back and forth through the beam. The hysteresis in the state machine even accommodates directional changes while a part is in the beam.

For the scheme to operate correctly, the object must be large enough to obscure both sensors. The sensors are used to control a synchronous state machine, and the object must move slowly enough that it does not obscure or clear both sensors within one clock period.

The bidirectionality of this scheme also makes it suitable for position sensing. The objects discussed above are replaced by a comb attached to some moving part. The part position is determined by counting the teeth on this comb as they pass through the light beam.

Operating Description

The state diagram of the counter controller is shown in Figure 2. Inputs A and B are High when the sensors are obscured. While no objects are present, the state machine holds in the Wait state. As an object moves into the beam, state variables S1 and S2 simply follow the inputs with a one clock delay. When the object exits the

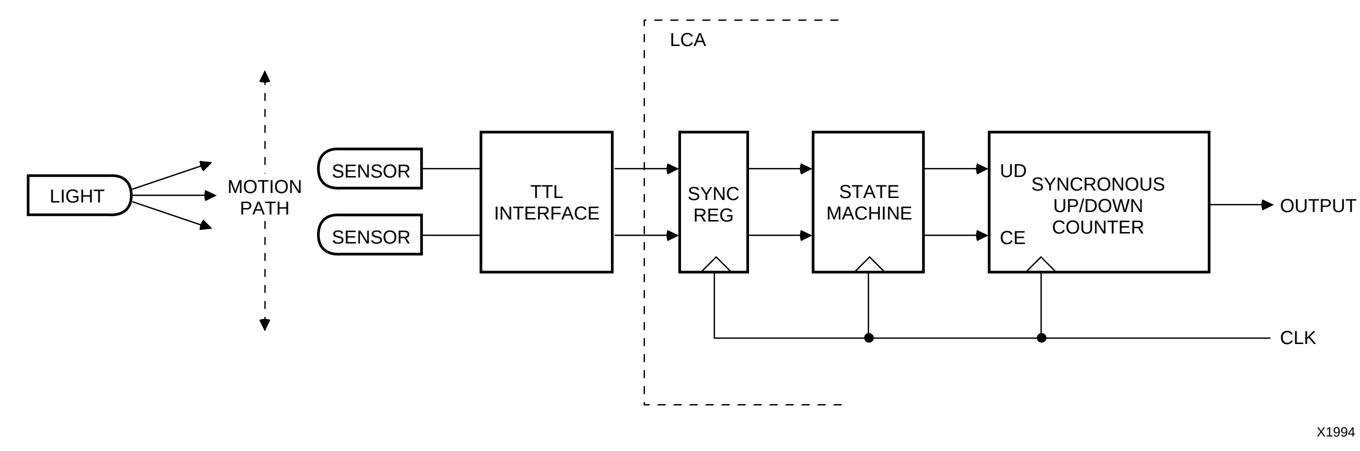
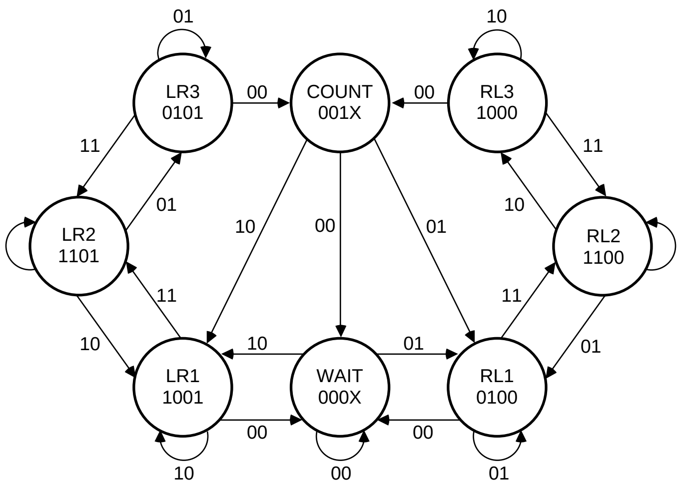


Figure 1. LCA Light-driven Counter



$S_1 = A$

$S_2 = B$

$S_3 = \bar{S}_1 \bullet S_2 \bullet S_4 \bullet \bar{A} \bullet \bar{B} + S_1 \bullet \bar{S}_2 \bullet \bar{S}_4 \bullet \bar{A} \bullet \bar{B}$ (COUNT ENABLE)

$S_4 = \bar{S}_1 \bullet \bar{S}_2 \bullet A + \overline{\bar{S}_1 \bullet \bar{S}_2} \bullet S_4$ (UP/DOWN)

Input AB
State Variables S_1 S_2 S_3 S_4

X2653

Figure 2. Light-driven Counter State Diagram

beam, the Count state is entered (S3 High) and the counter is enabled. One clock later, the state machine automatically moves out of the Count state and into the Wait state. If a new object is sensed from either direction during the Count state, the Wait state is omitted and the appropriate sequence commenced.

The identity of first sensor to be obscured is stored as the S4 variable. This is used to determine which sensor must be cleared last to ensure that the object has cleared the beam without reversing its direction. S4 also selects up or down operation of the counter. The up/down control is set up at least four clocks before the counter is enabled.

The state machine can be implemented in three CLBs, as shown in Figure 3. The asynchronous TTL-level signals are brought into the LCA device and registered in the IOBs. This synchronizes them to the state-machine clock and eliminates any metastability problems. S1 and S2 share a CLB. S3 is a function of five variables and requires a whole CLB. S4 occupies the third.

If required, the state machine implementation can be reduced to two CLBs. Using the DIN input, S1 can be combined with S3. S2 can then share the second CLB with S4.

Any synchronous up/down counter design may be used in conjunction with this state machine. The maximum count rate required is one fourth the clock rate.

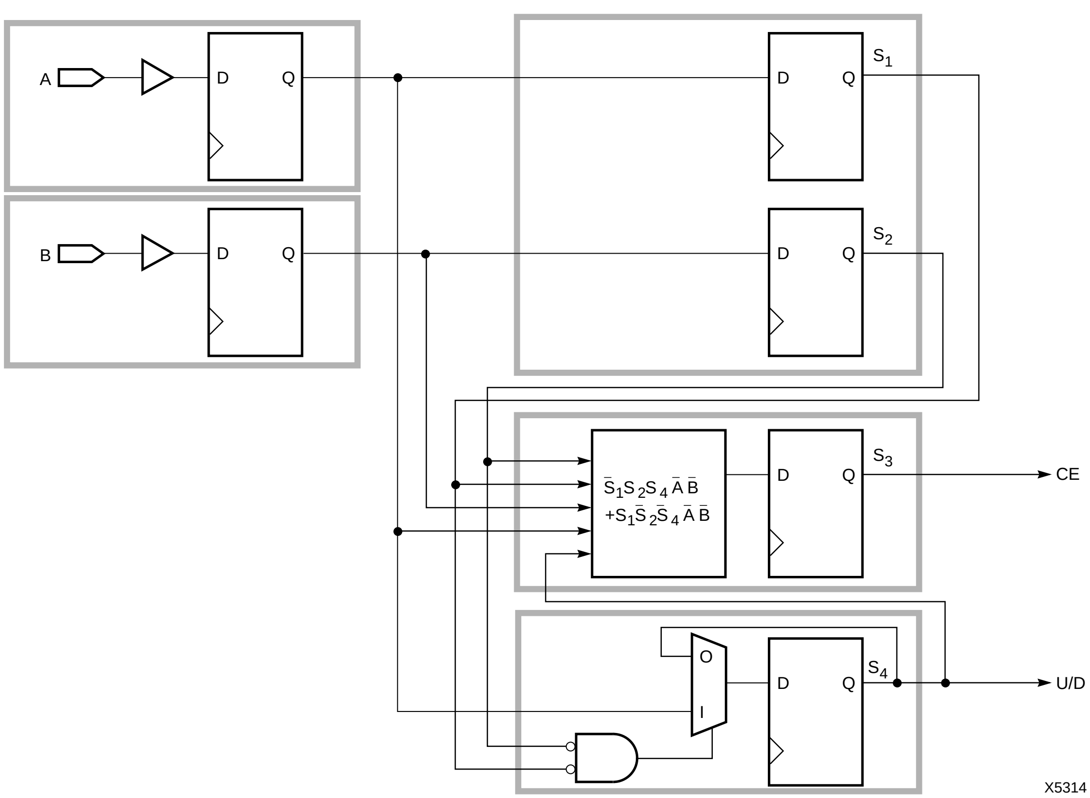


Figure 3. Light-driven Counter State Machine