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Obtaining Accurate Power Estimation for CoolRunner XPLA3 CPLDs Using XPower

Summary

Applications requiring low power components place the designer in the position of needing an accurate forecast of the power requirements of the system. These types of low power applications tend to be handheld, battery powered devices which are also inclined to be devices with short development cycles. Designers have discovered the advantage of using Xilinx CoolRunner™ XPLA3 CPLDs to both reduce power consumption and the development cycle of their system since the device is low power and reprogrammable. This document describes the technique used to more precisely predict the power consumption of CoolRunner XPLA3 CPLDs.

Power Basics

Xilinx CoolRunner CPLDs are true CMOS devices. Calculating power consumption in CMOS devices is relatively straight forward. CMOS devices consume power primarily in two ways: statically and dynamically.

Static current is a result of leakage current which flows through the channel of the transistor that is turned off. Ideally, this current is zero, but in reality is a fixed component of the total current.

Dynamic current is developed as a result of state switching of the CMOS device. Figure 1 illustrates dynamic current by using two cascaded CMOS inverters. Switching states causes two types of current to occur. First, during the transition, both the N-channel and the P-channel transistors are in the linear region where they both conduct, causing a brief spike in current from V_{DD} to GND as shown by the orange arrow in Figure 1. This transition current is relatively small since the transition time is very fast in the CoolRunner XPLA3 CPLDs. Second, depending on the previous state of the logic gate that these transistors comprise, this gates will either source or sink current to/from the next logic gate in the chain. MOSFET transistors are essentially capacitors when modeling gate impedance since the poly gate is simply a conductor on an oxide dielectric which, in turn, is on a conductive region of the channel. Also, there is a capacitive element developed from the routing throughout the die. Together, these capacitive components will charge and discharge through the previous logic gate's transistors as the previous gate switches states. The green arrow of Figure 1 shows current developed from charging and the blue arrow represents discharge. This flow of current is visible in the power pins of the CMOS device and comprises the dynamic component of the total current. Most dynamic current is derived from the capacitive charge and discharge since the transition

current is very small comparatively. Consequently, XPower combines these two components in the power model and represents dynamic current as the capacitive element to the user.

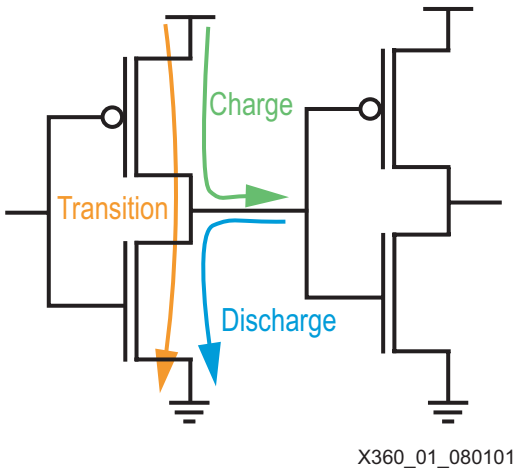

Figure 1: **Dynamic Current Through CMOS Inverters**

Total current, therefore, is the sum of the static current and the dynamic current. Since static current is a fixed component of the total current, it is only required to calculate the dynamic current. Dynamic current is simply the sum of the current generated during the state transitions of all logic gates in the device. This can be an overwhelmingly tedious task without the use of software and a few assumptions. This is where XPower becomes a necessity in the system design process.

Dynamic current is calculated as follows:

$$I = C \cdot V \cdot f$$

Where:

- **I** = current in Amperes
- **C** = capacitance in Farads
- **V** = device voltage in Volts
- **f** = transition frequency in Hz

Power is simply current multiplied again by voltage which yields Watts.

XPower Assumptions for CoolRunner XPLA3 CPLDs

To facilitate a power calculation in software, a few assumptions are made to provide reasonably accurate results and simplify the task:

- It is assumed that voltage applied to the device is constant and within the allowable range that the device is rated in the data sheet. It is up to the user to set the actual or estimated operating voltage.
- It is assumed that the device is operating within published timing and frequency limits. Entering a frequency outside of data sheet limits will yield results that are not accurate.
- Input transition times are 800 ps. XPower was correlated to a suite of designs in the lab where all input transition times were 800 ps. Transitions slower than 800 ps will result in higher power consumption in actual hardware implementation than what XPower will estimate. Therefore, for low power designs, it is advised to implement fast transition times on input singals.
- Logic components in the CPLD (e.g., product terms, etc.) are comprised of logic gates

which are constructed of CMOS transistors. Therefore, logic components within the device are assumed to be lumped capacitances consisting of smaller individual transistor capacitances.

With these assumptions, a device power model has been developed.

XPLA3 Power Model

Model Description

Prior to delving into a discussion that relies on knowledge of the XPLA3 architecture, it may be useful to review the CoolRunner XPLA3 Family Data Sheet found at http://www.xilinx.com/partinfo/ds012.pdf. Figure 2 shows a simplified representation of the power model for CoolRunner XPLA3 CPLDs. The model shows lumped capacitance values for specific architectural features. For example, a product term is comprised of many transistors and, in Figure 2, this is represented by the PT capacitance value shown in the AND gate.

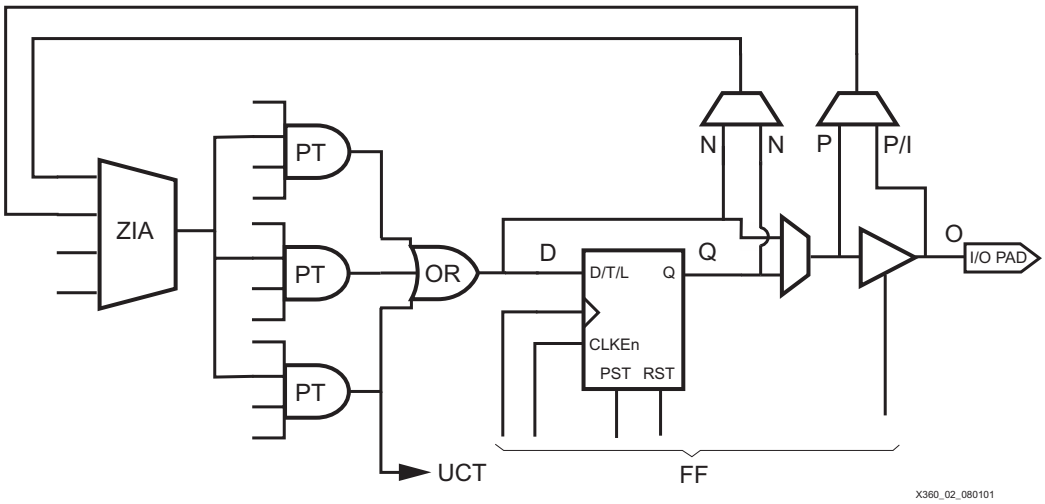

Figure 2: **Simplified Power Model for CoolRunner XPLA3 CPLDs**

These lumped capacitance values are displayed in the XPower Graphical User Interface (GUI) as a somewhat encoded net name. For example, a product term within Function Block #1 would be represented as FB1_PT12, where in this case the net is referring to product term #12. It is not necessary to know the internal arrangement of product terms, but product term numbers, for example, may be useful to determine the frequency of subsequent nets that rely on that product term.

Specific nets may be adjusted by the user to reflect the appropriate activity rate of those nets. Others are visible, but not available to the user for adjustment since the software updates the nets appropriately. An example of a net not available to the user for adjustment is ZIA. Nets that are available to the user to adjust are:

- **I** - Input net which is tied to an I/O pin
- **Q** - The net associated with the Q output of the flip-flop
- **D** - The net associated with the D input of the flip-flop but only when driven by the OR gate. If the D input is driven by a product term (PT), the net D will not be displayed in XPower.
- **N** - A feedback net to the ZIA which originates before the output buffer and obtains a source from either a combinatorial or registered signal
- **P** - A feedback net to the ZIA which originates either before or after the output buffer, depending on macrocell configuration
- **PT** - The output of a product term

Again, these nets are encoded into net names given by XPower. The above listed net designations follow identical nomenclature schemes with the exception of PT which was described earlier. An example of the nomenclature would be FB1_3_Q which refers to the Q output of the flip-flop which is associated with macrocell 3 located in Function Block 1. Similarly, FB4_12_I denotes the input net presented on the pin associated with macrocell 12 of Function Block 4.

As mentioned earlier, the activity rate of some nets, such as ZIA, are automatically adjusted by the software. A ZIA net will be denoted as FB1_ZIA_FB2_16_P, for example, where this is a net through the ZIA in Function Block 1. The source of the net is from Function Block 2, macrocell 16 and is the feedback net P shown in Figure 2. Another example of a net not available to the user is an OR net which would be denoted as FB1_7_OR. This is simply the sum-term tied to macrocell 7 of Function Block 1.

Power Consumption

Some elements of the power model consume more power than others. It is therefore vital to understand this since this will be key in reducing overall power consumption of the design. A user interested in further reducing power consumption will take into consideration which nets consume more power and accordingly either reduce the activity rate of those nets or avoid using those types of nets. It is also important to note that the higher power consuming elements demand accurate activity rate information to be entered in XPower to yield a more accurate power estimation. Below is a list of nets and their relative ranking of power consumption:

- **External Capacitance** - Very High
- **O** - High
- **UCT** - High - Larger with high density devices
- **I** - High - Larger with high density devices
- **P** - Medium - Somewhat larger with high-density devices
- **N** - Medium - Somewhat larger with high-density devices
- **ZIA** - Medium
- **PT** - Low
- **OR** - Low
- **FF** - Low
- **Q** - Very Low
- **D** - Very Low

Notice that External Capacitance is at the top of the list. External Capacitance is dominated by the trace capacitance on the board as well as capacitive loading of external devices connected to the net. Data sheets of these external components should list the capacitive loading of each pin on the device. Since the CoolRunner XPLA3 CPLD will source or sink current from external components, reducing external capacitive loading as well as external frequency will have a dramatic effect on overall power consumption of the CPLD.

Activity Rate

There are two basic types of activity rates that the user must address when entering data into XPower: Toggle Rate and Absolute Frequency. When referring to both types, the term Activity Rate will be used throughout the document.

Absolute Frequency

The first type of activity rate is entered into the GUI as an absolute frequency expressed in MHz. Nets requiring this type of activity rate will be referred to as absolute frequency. All nets in the CoolRunner XPLA3 CPLD design will use absolute frequency except for Q nets driven by a global clock. Q nets driven by a product term clock require absolute frequency to be set.

Toggle Rate

A Q net that is associated with a clock, but not a product term clock, will require its activity rate to be entered as a toggle rate which is relative to the clock frequency driving that net. Product term clocks will require absolute frequency to be given by the user. Toggle Rates are entered as a percentage of the clock frequency driving the flip-flop. This rate is related only to the active edge of the clock. A toggle rate of 100% indicates that the Q output will change states on every active clock edge.

For example, a Q net named FB1_3_Q which is associated with a T type flip-flop whose T input is held High will transition at half the frequency of the clock. Assuming, in this example, the clock is active High, the Q output will change state on every rising edge of the clock resulting in half the frequency of the clock. Therefore, the net in this example would require a 100% toggle rate.

It may be somewhat easier to grasp this concept by thinking in terms of active edges of the clock in lieu of frequencies.

The user must enter into the GUI toggle rates as a percentage value. Once the number has been entered into the field associated with the net, the number will change and be displayed as absolute frequency, in units of MHz, relative to the clock frequency.

Toggle Rates are very useful to the user in what-if scenarios. Once all absolute frequencies and toggle rates have been given by the user, it is simple to see the change in power consumption by adjusting clock frequencies. Changing a clock frequency will result in all Q nets changing displayed frequency which is based on toggle rates. This avoids the requirement to adjust all nets that depend on the clock, resulting in a tool with greater ease of use.

Data Entry Methods

There are several methods to enter the activity rates of the nets in the design. Each method has its advantages and shortfalls. Listed below are the usual methods listed in order of most tedious data entry at the top to the least tedious at the bottom.

- Hand entry
- Estimate Activity Rates
- Simulation using Model Technology™ ModelSim®

Data Entry By Hand

Manual data entry is the most accurate method currently possible for XPower. However, intimate knowledge of the design in question and CoolRunner XPLA3 CPLD architecture is required for accurate results which, by its very nature, will be the most tedious method. Since the other two methods, described below, involve estimation of activity rates, this will be the most accurate method. As the saying goes, "Garbage in, garbage out", therefore it is important that the activity rates entered into XPower are correct for the design. It is imperative that the user specify a toggle rate or absolute frequency for all nets. Any nets left at the default value will cause the power estimation to be inaccurate.

XPower has a useful feature in the Tools menu called "Estimate Activity Rates". Those nets that cannot be changed by hand entry must have their activity rates set by this feature.

Determining the activity rate of all nets existing in the design is not a trivial task, but depending on the design, this may be a possible approach. For example, a counter is very predictable regarding the activity rates of the nets within the design. In cases like this it may be advantageous to determine the activity rates of all internal nets. Another example is an address decoder which may have predictable activity rates, depending on the application.

Designs that are more complex, for example those involving state machines, may be nearly impossible to determine the activity rates of all nets by hand. For these types of designs, the other two methods described below may be preferred.

Estimate Activity Rates

The Estimate Activity Rates feature can be used in conjunction with partial data entry by hand, as described above, to reduce the tedious nature of the task. XPower uses an algorithm to determine the absolute frequencies of those nets that have not yet been set by the user, thereby alleviating the burden on the user to specify absolute frequencies for all nets. Since an algorithm is employed, the frequencies predicted may not reflect actual frequencies, thereby introducing inaccuracies in the estimation. Therefore, this method is not as precise as editing all activity rates by hand.

"Estimate Activity Rates" only estimates absolute frequencies, not toggle rates. In other words, the algorithm does not estimate the Q output toggle rates of registers. It will only change the absolute frequencies for combinatorial nets. Recall that toggle rates are only used for Q outputs of flip-flops and are percentages of the clock frequency.

Using this method, it is necessary to edit by hand all primary I/Os and all buried registers with realistic activity rates to obtain the most realistic activity rate estimation for the remaining nets. Once "Estimate Activity Rates" has been utilized, it will be apparent in the GUI which nets have not yet been set since they will remain at the default value. These remaining nets will be dependent on other nets that have been neglected by the user.

Primary I/O activity rate information should be known to the user and therefore should be a trivial task to enter this data into XPower. It may not be known at what activity rate the buried registers change states. In this case simulation using ModelSim may be a more viable solution.

Recommended Flow

To use this method, follow these steps to ensure data is retained as intended:

1. Edit primary inputs, I/O, and buried registers by hand. This step requires that the Q output of all registers have been checked to have correct toggle rates.
2. Apply Estimate Activity Rates

Implementing a flow that is in any other order than that described here will likely result in inaccurate results.

Simulation using ModelSim

Of the three methods listed in this note, simulation is by far the easiest method. This method requires simulation of the design using ModelSim. The Xilinx starter version of ModelSim XE is available free of charge from the Xilinx website at **http://www.xilinx.com/sxpresso/webpack.htm**.

Using ModelSim, the user can create a Value Change Dump (VCD) file containing transition data noted during the simulation. This VCD file is imported into XPower which then converts the data to activity rate data and is matched to the appropriate net.

It is important to note that a simulation must be of sufficient length. Otherwise, signals that change states very infrequently will be misrepresented in the VCD file. For example, a reset signal may not be used much in the design, which may yield an unreasonably high activity rate and high power estimation. If, for example, the reset signal is used once every five seconds and the simulation only lasted 500 ms, the signal only changed state one time. The VCD file may represent this as a activity rate orders of magnitude too high. In this example, the simulation must last at least five seconds, or preferably longer, to more accurately capture the activity rate of this seldom used reset signal. Inspect all nets for expected activity rates and then ensure that the simulation time is of sufficient length to retain valid activity rate information for all nets.

The current version of XPower can only use the top level nets listed in the VHDL or Verilog designs. Nets listed in lower levels of the hierarchy will not be used by XPower. Therefore, it is necessary to modify by hand the activity rates of those nets listed in XPower that were not included in the VCD file. It is recommended that primary I/Os and buried registers that have not been captured by the VCD file be edited by hand to reflect the true activity rate. If it is not readily apparent what activity rate these types of nets require, it can be obtained from a subsequent simulation. Simply add those nets to the simulation and run again, but do not create another

VCD file since this would overwrite the existing file. Once simulation is complete, it can be determined from the Signals window the average activity rate for each net in question.

After the primary I/O and buried register data have been entered into the GUI by using the VCD file and by hand editing the data, it is necessary to apply the "Estimate Activity Rates" tool. Doing so will ensure all remaining nets obtain activity rates.

As mentioned earlier, this method is the easiest to implement. It is not as accurate as the brute force method of hand entry, but may be a bit more accurate than the Estimate Activity Rates method mentioned above. Since the simulator contains timing information necessary to propagate signal transitions, the activity rates of all nets are accurately represented.

Recommended Flow

For simulation using ModelSim follow these steps to ensure data is retained as intended:

1. Generate VCD file
2. Edit primary inputs, I/O, and buried registers by hand. Optionally adjust activity rates of those provided by the VCD file to ensure proper data. This step requires that the Q output of all registers have been checked to have correct toggle rates.
3. Apply Estimate Activity Rates

Implementing a flow that is in any other order than that described here will likely result in inaccurate results.

Improving Accuracy

Capacitive Loads

Power consumption of any device is not limited to the circuitry of the die, but is also mandated by the capacitance of the trace on the printed circuit board and any external devices connected to that I/O pin. Current required to charge and discharge the external capacitance is derived from the power pins of the device. Consequently, this current is added to the current required to operate the internal circuitry of the device which results in a higher total power consumption. Regardless of whether the device is a low power CoolRunner CPLD or a more power hungry device, external capacitive loading will have a dramatic effect on overall power consumption. It is therefore recommended to reduce the external load capacitance to lower power consumption.

XPower can calculate and display by what amount external capacitive loading affects power. It is vital to either measure or calculate external capacitive loading to provide reasonable data to XPower for a valid calculation. The absolute frequency described on the O net will be applied against external capacitance in the calculations, therefore an accurate representation of the output buffer absolute frequency is needed for a reasonable value of power consumption.

Macrocell Configurations

A better understanding of the XPLA3 power model is required to improve the results of the power estimation given by XPower. The discussion that follows is mostly applicable to the data entry by hand method since it is vital to enter all net activity rates accurately.

The other methods involve applying the activity rate estimator which inherently determines the appropriate activity rates for those listed in the power model. When using these other methods, provided all primary I/O and buried register activity rate data has been correctly entered, it is only necessary to perform a quick check regarding the discussion below to ensure that all nets have been appropriately addressed.

This discussion involves macrocell configurations and correlation to the power model. It is not useful to discuss the ZIA since the Estimate Activity Rates tool treats the ZIA as a non-inverting buffer. Therefore absolute input frequencies equal output frequencies. Consequently, it is important to specify the correct activity rates to the macrocell outputs or I/O input pins.

Nor is it possible to discuss the PLA since the user does not have access to product term or sum term numbers. In other words, there is no publicized cross reference from fitter report to

product term/sum term numbers. It is vital to use the Estimate Activity Rates tool within XPower to apply activity rates to these elements.

Given that all primary I/Os and input activity rates have been set by the user, below is a list of nets for which the Estimate Activity Rates tool will calculate activity rates:

- **UCT**
- **O** - based on output pin absolute frequency
- **I** - based on input pin absolute frequency
- **P**
- **N**
- **ZIA** - based on N or P absolute frequency
- **PT**
- **OR**
- **FF**
- **D** - based on OR gate absolute frequency

Some nets cannot use the Estimate Activity Rates tool and these are listed below:

- **External Capacitance**
- **Q**

Several macrocell configurations are possible with CoolRunner XPLA3 CPLDs. To gain a better understanding of these types of configurations, it is advised to review the Macrocell Configurations in CoolRunner XPLA3 CPLDs application note found at http://www.xilinx.com/xapp/xapp335.pdf. This discussion will rely heavily on this application note.

Combinatorial Output

The macrocell can be configured as combinatorial driving an I/O pin. Figure 3 shows what path the signal takes through the macrocell.

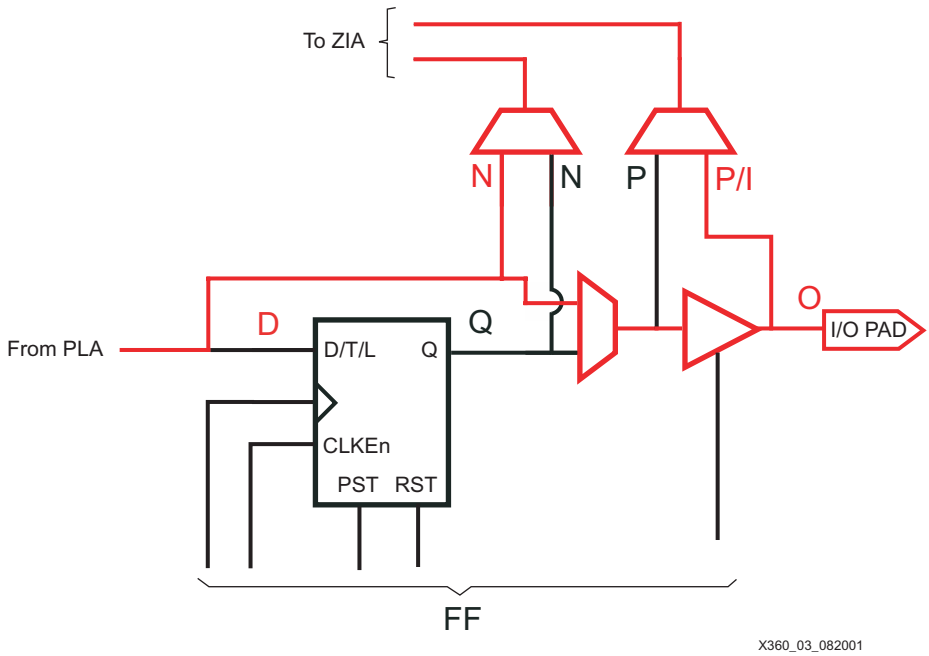

Figure 3: **Combinatorial Output Data Path**

Nets shown in red are those that must be assigned an absolute frequency. Specifically:

- **N** - Absolute frequency

- **P** - Absolute frequency. This net may not appear in the GUI depending on the type of feedback used.
- **O** - Automatically entered by XPower based on absolute frequency specified on the I/O pin
- **D** - Adjusted by Estimate Activity Rates as an absolute frequency and is based on output of OR term

All nets in this configuration will have the same absolute frequency.

Registered/Latched Output

CoolRunner XPLA3 CPLDs can have the macrocell configured as either a Latch, D, or T type of flip flop. Figure 4 shows the data path with this type of configuration.

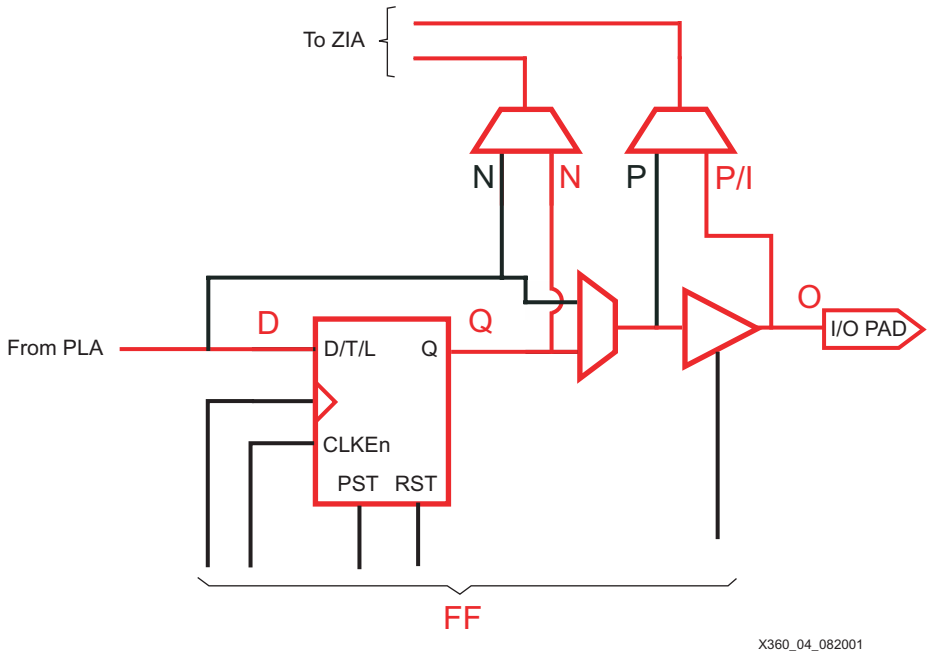

Figure 4: **Registered/Latched Output Data Path**

The following nets must have activity rates set:

- **Q** - Toggle Rate
- **N** - Absolute frequency
- **P** - Absolute frequency. This net may not appear in the GUI depending on the type of feedback used.
- **D** - Adjusted by Estimate Activity Rates as an absolute frequency and is based on output of OR term
- **O** - Automatically entered by XPower based on absolute frequency specified on the I/O pin

Nets N, P, and O will have the same absolute frequency as the resultant frequency of Q, which in turn is dictated by the toggle rate specified by the user. Net D will reflect the same absolute frequency as the OR term that drives it, and therefore will be automatically adjusted by Estimate Activity Rates.

Combinatorial Node

Macrocells that do not drive an I/O pin are nodes. There are two possible cases where nodes exist. First, a net from a macrocell is specified to be a node by the design or the fitter, and

second, the macrocell is simply not bonded to a pin. Figure 5 shows how this correlates to the power model for XPLA3 CPLDs.

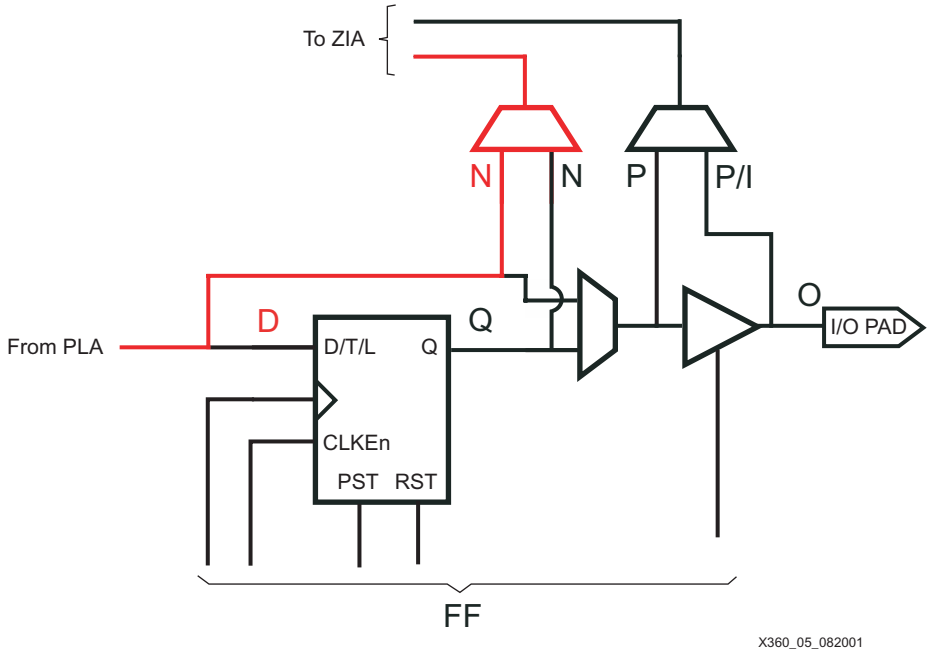

Figure 5: **Combinatorial Node Data Path**

Combinatorial nodes require attention to the following nets:

- **N** - Absolute Frequency
- **D** - Adjusted by Estimate Activity Rates as an absolute frequency and is based on output of OR term

All nets have the same absolute frequency with this arrangement.

Registered/Latched Node

Similar to Combinatorial Node configurations, registered or latched macrocells can be configured as nodes. Figure 6 displays this type of configuration and the associated data path through the power model for XPLA3 CPLDs.

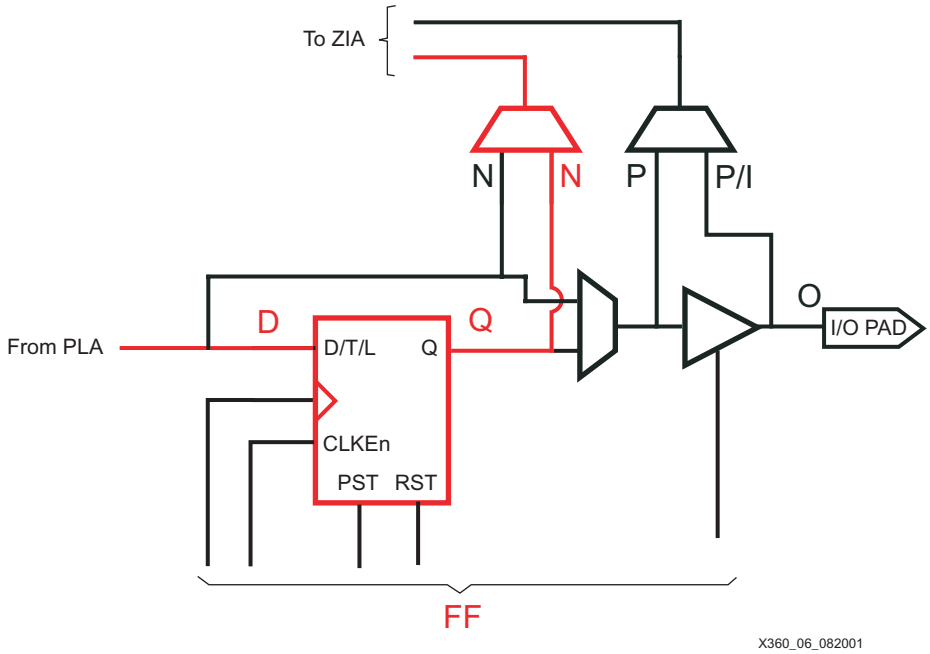

Figure 6: **Registered/Latched Node Data Path**

This configuration requires activity rates applied to the following nets:

- **Q** - Toggle rate
- **N** - Absolute frequency
- **D** - Adjusted by Estimate Activity Rates as an absolute frequency and is based on output of OR term
- **FF** - Automatically entered by XPower as an absolute frequency

Net N will have the same absolute frequency as the resultant frequency of Q, which in turn is dictated by the toggle rate specified by the user. Net D will reflect the same absolute frequency as the OR term that drives it, and therefore will be automatically adjusted by Estimate Activity Rates.

Input Only

Macrocells can be configured such that the output buffer is 3-stated which makes the I/O pin function as an input. In this case, the data path is shown in Figure 7.

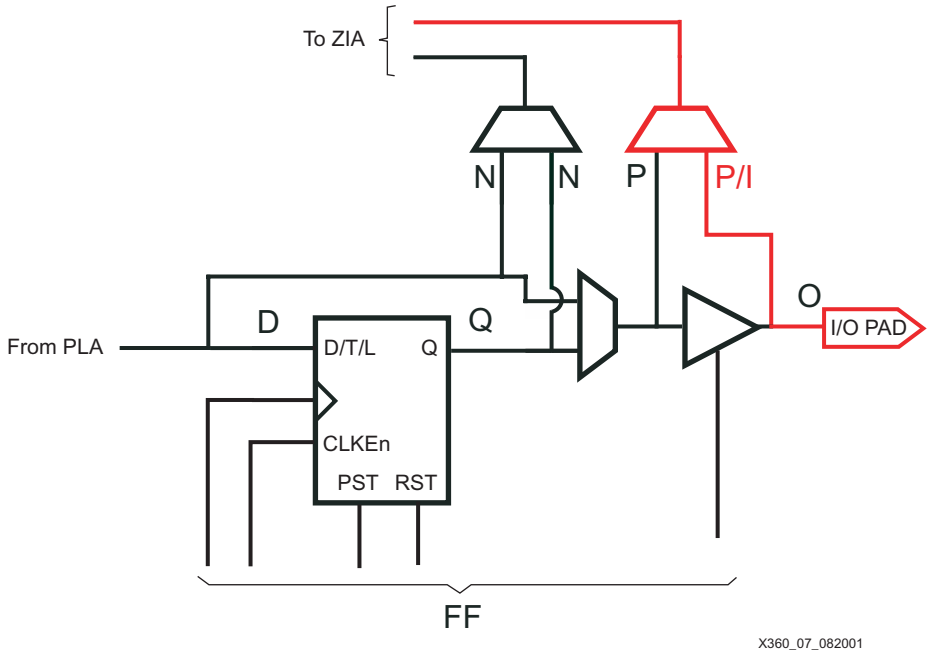

Figure 7: **Input Only Data Path**

Macrocells configured as an input require the following nets activity rates to be defined:

- **I** - Absolute frequency
- **P** - Absolute frequency

Nets I and P will have the same absolute frequency as the input signal.

Input with Combinatorial Node

When a macrocell is configured as a node, the output buffer is 3-stated. This permits the designer to use the I/O pin as an input. When the XPLA3 CPLD is configured in this fashion, the combinatorial node and input signals take the paths shown in Figure 8.

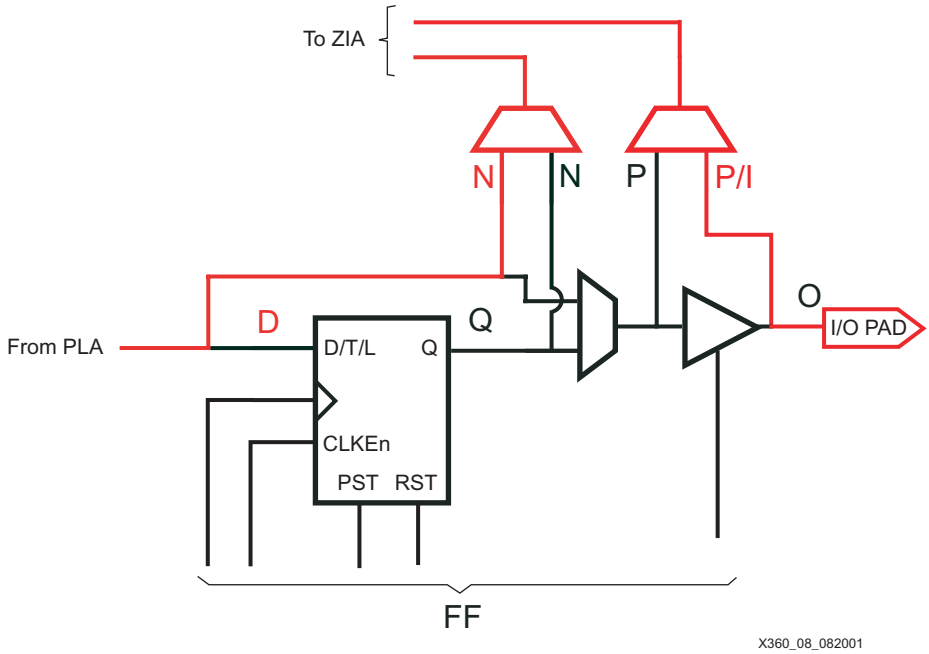

Figure 8: **Input with Combinatorial Node Data Path**

This type of configuration requires activity rates applied to the following nets:

- **N** - Absolute frequency
- **I** - Absolute frequency
- **P** - Absolute frequency
- **D** - Adjusted by Estimate Activity Rates as an absolute frequency and is based on output of OR term

Nets D and N will have the same absolute frequency. Nets I and P will reflect the absolute frequency of the input net driving the I/O pin.

Input with Registered/Latched Node

Similar to Input with Combinatorial Node, the macrocell can be configured to be a register or latch while making available the I/O pin as an input. Figure 9 describes the data flow in this situation.

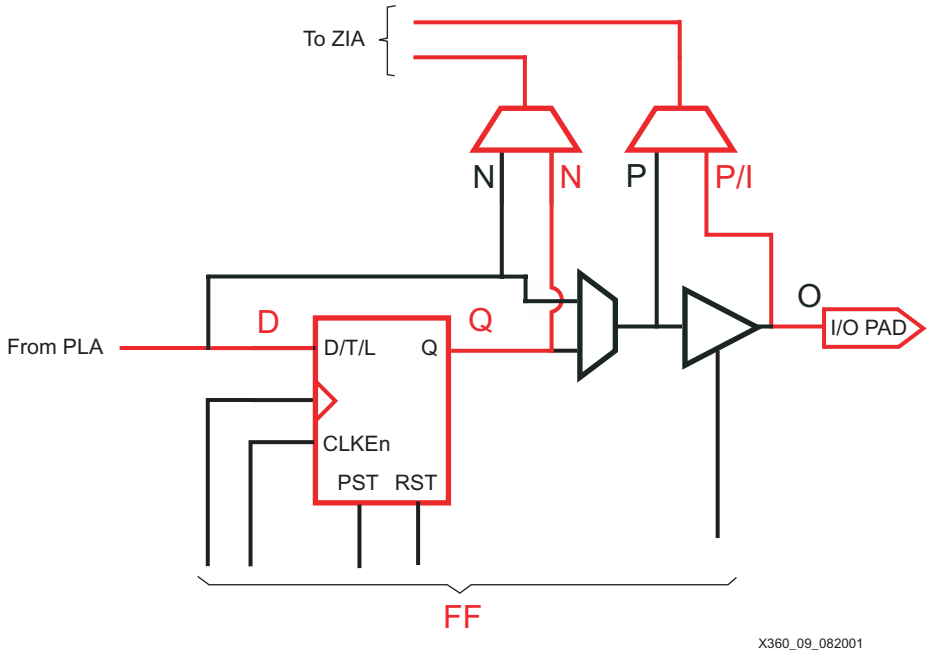

Figure 9: **Input with Registered/Latched Node Data Path**

Macrocells with this configuration must have the following nets addressed:

- **Q** - Toggle Rate
- **N** - Absolute frequency
- **I** - Absolute frequency
- **P** - Absolute frequency
- **D** - Adjusted by Estimate Activity Rates as an absolute frequency and is based on output of OR term
- **FF** - Automatically entered by XPower as an absolute frequency

Nets Q and N must have the same absolute frequency once toggle rate has been set for Q. Nets I and P will reflect the absolute frequency of the input net driving the I/O pin.

Input Register

The CoolRunner XPLA3 CPLD macrocell can be configured as an input register with fast setup times. The I/O pin is directed to the input of the flip-flop in a direct manner that bypasses the ZIA and the PLA. This greatly reduces setup time which allows pipelining, thereby increasing board clock speed. Figure 10 demonstrates the input register configuration. The dashed red line

shows the input signal data path from the I/O pin directly to the input of the flip-flop. The solid red line shows the data path from the flip-flop output to the ZIA.

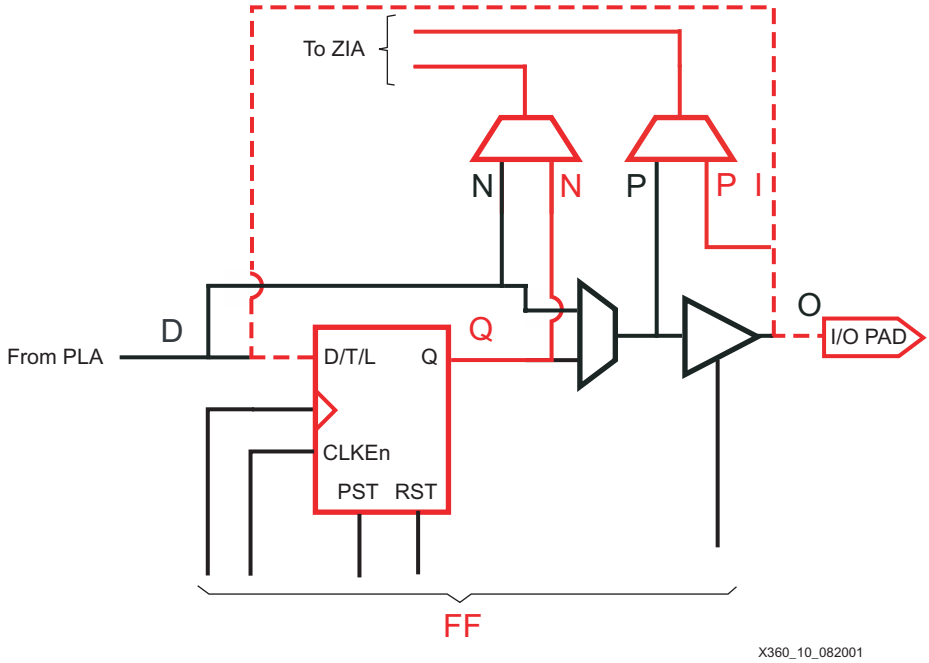

Figure 10: **Input Register Data Path**

The following nets must have their activity rates set for Input Register configurations:

- **Q** - Toggle rate
- **N** - Absolute frequency
- **I** - Absolute frequency
- **P** - Absolute frequency
- **FF** - Automatically entered by XPower as an absolute frequency

Net N will have the same absolute frequency as the resultant frequency of Q, which in turn is dictated by the toggle rate specified by the user. Nets I and P will reflect the same absolute frequency as the input signal on the I/O pin.

Input Register with Combinatorial Node

To further utilize the macrocell in XPLA3 CPLDs, the designer may place a combinatorial node on a macrocell configured as a fast input register. Figure 11 shows this implementation where the green data path represents the combinatorial node. Again, the dotted red line represents

the data path of the input signal applied to the I/O pin. The solid red line denotes the data path from the output of the flip-flop to the ZIA.

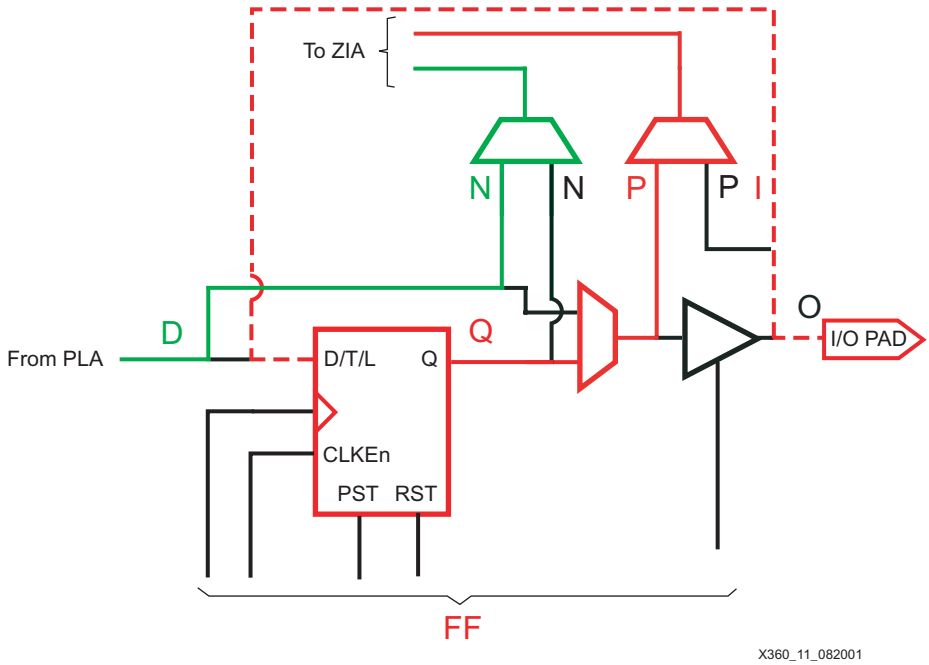

Figure 11: **Input Register with Combinatorial Node Data Path**

Activity rates must be applied to the following nets when the macrocell is configured as an input register with a combinatorial node:

- **Q** - Activity rate
- **N** - Absolute frequency
- **P** - Absolute frequency
- **I** - Absolute frequency
- **D** - Adjusted by Estimate Activity Rates as an absolute frequency and is based on output of OR term
- **FF** - Automatically entered by XPower as an absolute frequency

Net I will be the same absolute frequency as the input signal applied to the I/O pin. Net P will have the same absolute frequency as the resultant frequency of Q, which in turn is dictated by the toggle rate specified by the user. Nets D and N will have the same absolute frequency since these nets represent the combinatorial node. Net D will reflect the same absolute frequency as the OR term that drives it, and therefore will be automatically adjusted by Estimate Activity Rates.

Bi-directional, Combinatorial

Macrocells configured as combinatorial with bi-directional I/Os are represented in Figure 12. Although the data path through the power model for XPLA3 CPLDs looks similar to the combinatorial macrocell in Figure 3, this type of configuration requires special consideration.

The data path through the P net (shown in blue) may have a different absolute frequency compared to the O net (shown in green), depending on the application. Since O represents the output buffer, it will only be toggling when the output buffer is enabled. Therefore, power consumption of the output buffer will be less than if it were enabled 100% of the time. By the same token, the P net will be switching at the same rate as the O net, but only when the output buffer is enabled. Otherwise, the P net will be switching at the same rate as the input signal presented to the I/O pin.

To obtain maximum accuracy, it is recommended to treat the P net as the average absolute frequency between the two cases of the output buffer: enabled and disabled. It is important to take the duty cycle of the output buffer enable signal into consideration to weight the average absolute frequency. It is also suggested that the absolute frequency of the O net represent the average absolute frequency of the output signal, adjusted for the amount of time the output buffer is enabled as dictated by the output enable duty cycle.

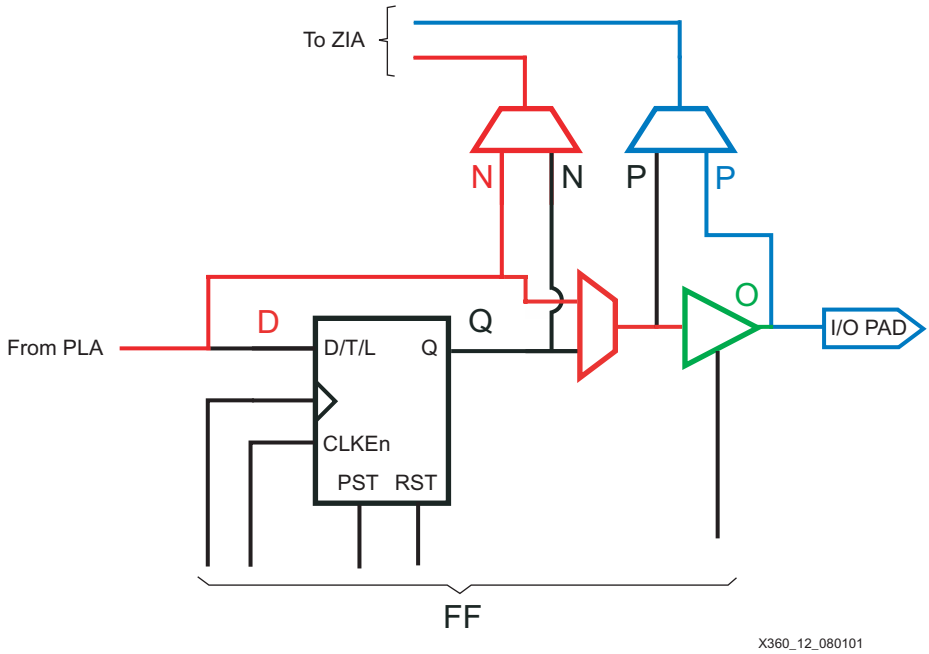

Figure 12: **Bi-directional, Combinatorial Data Path**

Nets to be considered are:

- **N** - Absolute frequency
- **P** - Weighted absolute frequency, depending on output enable duty cycle, input and output absolute frequency
- **O** - Automatically entered by XPower based on absolute frequency specified on I/O pin
- **D** - Adjusted by Estimate Activity Rates as an absolute frequency and is based on output of OR term

Nets N and D will have the same absolute frequency but may differ from the O net since the output buffer may not be enabled 100% of the time.

Net O will have the same absolute frequency as the output net named in the user's design file. For example, if the output net was named DATA0, which switches at 10 MHz as an output signal where the output buffer is enabled 75% of the time, set DATA0 to 7.5 MHz. Net O will automatically be set to 7.5 MHz by XPower. Again, output signals will have an absolute frequency that is equal to or less than the N and D nets, depending on the amount of time the output buffer is enabled.

Similarly, with the above example, DATA0 switches at 20 MHz as an input signal with the output buffer disabled for 25% of the time. Set the P net to 12.5 MHz which is 5 MHz (input) + 7.5 MHz (output).

Bi-directional, Registered/Latched

This type of configuration is nearly identical to the bi-directional, combinatorial macrocell. Figure 13 displays the data paths involved with this configuration, with blue representing the input net and green the output net. Refer to the previous section for more details.

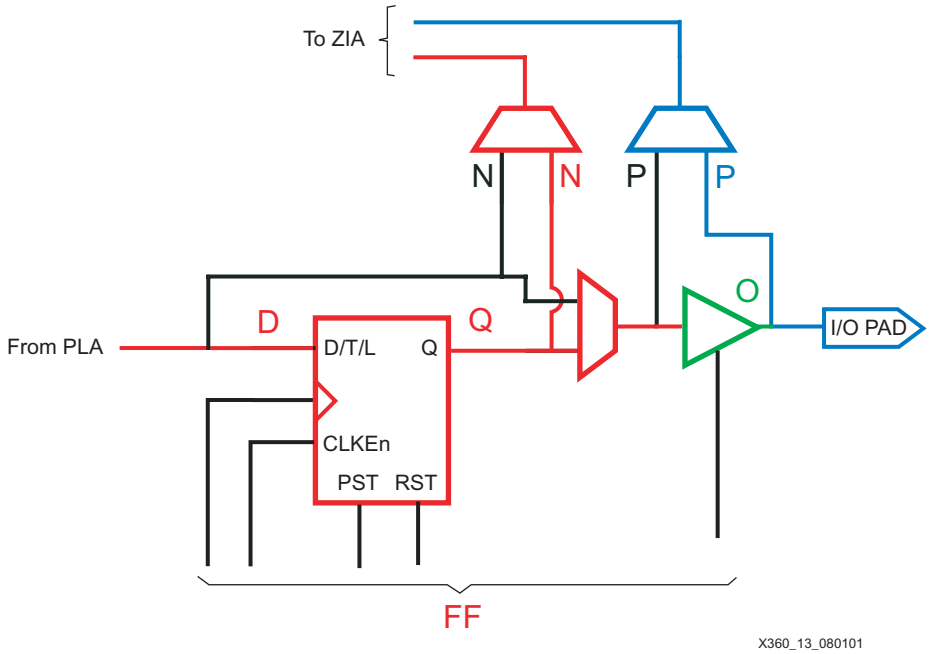

Figure 13: **Bi-directional, Registered/Latched Data Path**

Nets requiring consideration are:

- **N** - Absolute frequency
- **Q**- Activity rate
- **P** - Weighted absolute frequency, depending on output enable duty cycle, input and output absolute frequency
- **O** - Automatically entered by XPower based on absolute frequency specified on I/O pin
- **D** - Adjusted by Estimate Activity Rates as an absolute frequency and is based on output of OR term
- **FF** - Automatically entered by XPower as an absolute frequency

Nets N and Q will have the same absolute frequency as determined by the toggle rate of Q, but may differ from net O since the output buffer may not be enabled 100% of the time.

As described earlier, net O will have the same absolute frequency as the output net named in the user's design file. For example, if the output net was named DATA0, which switches at 10 MHz as an output signal where the output buffer is enabled 75% of the time, set DATA0 to 7.5 MHz. Net O will automatically be set to 7.5 MHz by XPower. Again, output signals will have an absolute frequency that is equal to or less than the N and Q nets, depending on the amount of time the output buffer is enabled.

Similarly, with the same example, DATA0 switches at 20 MHz as an input signal with the output buffer disabled for 25% of the time. Set the P net to 12.5 MHz which is 5 MHz (input) + 7.5 MHz (output).

Summary

Designers who are constrained by power supply requirements or those that are concerned with system thermal limits can benefit from the use of XPower. The tool provides accurate power, current, and thermal calculations when the correct data is applied to the design. Although

tedious data entry by hand yields the most accurate power calculation, it is not necessarily the method of choice. Simulation using ModelSim is, by far, the preferred method since it is quick and quite accurate. In addition, simulation reduces the possibility of data entry error. Regardless of the data entry method used, XPower provides a method for generating improved power consumption estimates.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
08/15/01	1.0	Initial Xilinx release.