Using the XC9500XV Timing Model

XAPP362 (v1.0) August 20, 2001

Summary

This application note describes how to use the XC9500XV timing model.

Introduction

All XC9500XV CPLDs have a uniform architecture and an identical timing model, making them very easy to use and understand. To determine specific timing details, users need only compare their paths of interest to the architectural diagrams and, using the timing model presented here, perform a simple addition of incremental time delays.

Device Timing Overview

External signals arrive at the pins and are delivered through the I/O block to the FastCONNECT™ II Switch Matrix. From the switch matrix, they are dispatched to the various Function Blocks (FBs). As the signals enter the FBs, they incur incremental time delays depending on how the signals are used within the FB. For example, all logic signals must pass through the AND array where they encounter product terms which add a time delay as the signals progress. Additional time delay may be encountered if the signals pass through the cascade logic and are redirected toward macrocells that are farther away than those directly attached to the product terms.

There are additional timing requirements such as setup and clock-to-output times involved with passing signals through a flip-flop. As the signals exit flip-flops, they either pass to the outside world, through the I/O pins, or are fed back into the FastCONNECT II switch matrix for additional logic operations.

Design timing can be manually analyzed as separate signals, each having unique timing parameters that are easily calculated. However, the Xilinx software provides a detailed timing report that tallies and summarizes all paths specified by the designer. The timing report is based on the model described here and is a convenient text based mechanism for isolating and displaying timing relationships.

The timing model shown in Figure 1 is used by the Xilinx development software which provides complete fitters for the XC9500XV family as well as the timing models for simulation and detailed static timing reports.

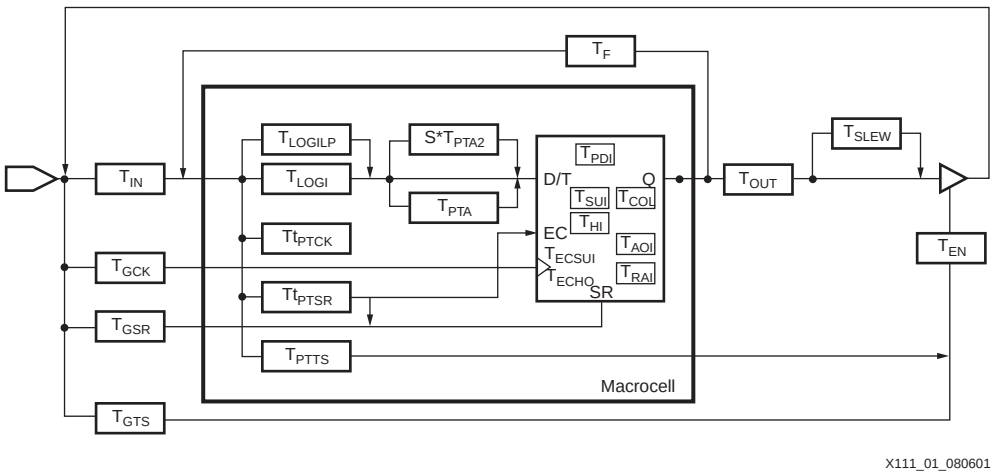


Figure 1: **XC9500XV Detailed Timing Model**

Timing Model

The timing model shown in Figure 1 resembles the XC9500XV macrocell with additional time delays included to account for the FastCONNECT II Switch Matrix and I/O buffers. As signals progress through an XC9500XV device, they encounter each of these delays which are tallied to arrive at a cumulative time delay for that signal. Table 1 provides a detailed definition of each parameter contained in Figure 1. The exact values of these parameters for each device can be obtained from the specific data sheets.

Table 1: **Key XC9500XV Timing Parameter Definitions**

Symbol	Parameter
Buffer Delays	
T_{IN}	Input buffer delay
T_{GCK}	GCK buffer delay
T_{GSR}	GSR buffer delay
T_{GTS}	GTS buffer delay
T_{OUT}	Output buffer delay
T_{EN}	Output buffer enable/disable delay
Product Term Control Delays	
T_{PTCK}	Product term clock delay
T_{PTSR}	Product term set/reset/clock-enable delay
T_{PTTS}	Product term 3-state delay
Internal Register and Combinatorial Delays	
T_{PDI}	Combinatorial logic propagation delay
T_{SUI}	Register setup time
T_{HI}	Register hold time
T_{COI}	Register clock to output valid time
T_{AOI}	Register async. S/R to output delay
T_{RAI}	Register async. S/R recovery before clock
T_{LOGI}	Internal logic delay
T_{LOGILP}	Internal low power logic delay
T_{ECSUI}	Register setup for clock enable
T_{ECHO}	Register hold for clock enable
Feedback Delays	
T_F	FastCONNECT II matrix feedback delay
Time Adders	
T_{PTA}	Initial product term allocator delay
T_{SLEW}	Slew rate limited delay
T_{PTA2}	Additional product term allocator delay

Timing Calculation Examples

Table 2 shows how various external timing parameters are derived from the internal timing parameters. For example, T_{PD} is the sum of the input buffer time delay (T_{IN}), the logic time delay (T_{LOGI}), the flip-flop pass through delay (T_{PDI}), and the output buffer time delay (T_{OUT}), as shown in Figure 2. Note that the input buffer delay is combined with the time delay accrued when the entering signal passes through the FastCONNECT II switch matrix.

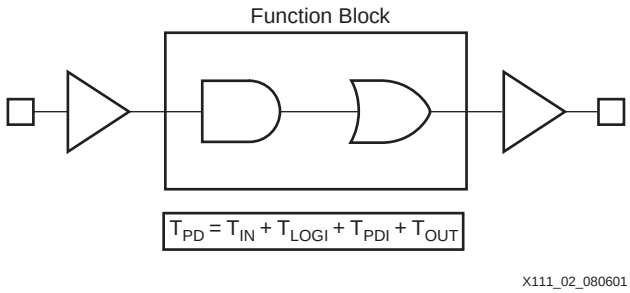


Figure 2: **Simple T_{PD} Example**

Table 2: **Expressions for Key Timing Parameters Derived from Table 1**

Symbol	Parameter	Calculation
T_{PD}	Propagation delay	$T_{IN} + T_{LOGI} + T_{PDI} + T_{OUT}$
T_{SU}	Global clock setup time	$T_{IN} + T_{LOGI} + T_{SUI} - T_{GCK}$
T_{H}	I/O hold time after GCK	$T_{GCK} + T_{HI} - T_{IN} - T_{LOGI}$
T_{CO}	Global clock-to-output	$T_{GCK} + T_{COI} + T_{OUT}$
f_{SYSTEM}	Internal system clock period	$1/(T_{COI} + T_{F} + T_{LOGI} + T_{SUI})$
T_{PSU}	P-term Clock setup time	$T_{IN} + T_{LOGI} + T_{SUI} - T_{IN} - T_{PTCK}$
T_{PH}	I/O hold time after p-term clock	$T_{IN} + T_{PTCK} + T_{HI} - T_{IN} - T_{LOGI}$
T_{PCO}	Product term clock-to-output	$T_{IN} + T_{PTCK} + T_{COI} + T_{OUT}$
T_{ECSU}	Clock enable setup time	$T_{IN} + T_{PTSR} + T_{ECSUI} - T_{GCK}$
T_{ECH}	Clock enable hold time	$T_{GCK} + T_{ECHO} - T_{IN} - T_{PTSR}$
T_{OE} T_{OD}	GTS to output enabled/disabled	$T_{GTS} + T_{EN}$
T_{POE} T_{POD}	P-term OE to output enabled/disabled	$T_{IN} + T_{PTTS} + T_{EN}$

Figure 3 shows a variation on the simple T_{PD} example with the addition of cascaded product terms. The time delay from input A is slightly altered by the addition of T_{PTA}. The XC9500XV can accept and deliver product terms in both directions with the same T_{PTA} delay. Also, product terms may arrive from non-adjacent macrocells, which would require an additional T_{PTA2} to be added for each macrocell hop. The design implementation software may incur multiple cascade

delays as required to fit the design. This cascade timing can be managed by using timing driven optimization in the Xilinx CPLD software.

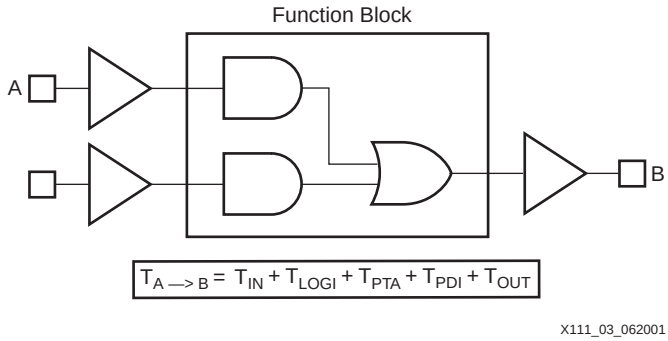


Figure 3: **T_{PD} with Initial Cascaded P-Terms**

Figure 4 shows how T_{PD} is derated with an inital cascade delay and a subsequent one from a more distant macrocell.

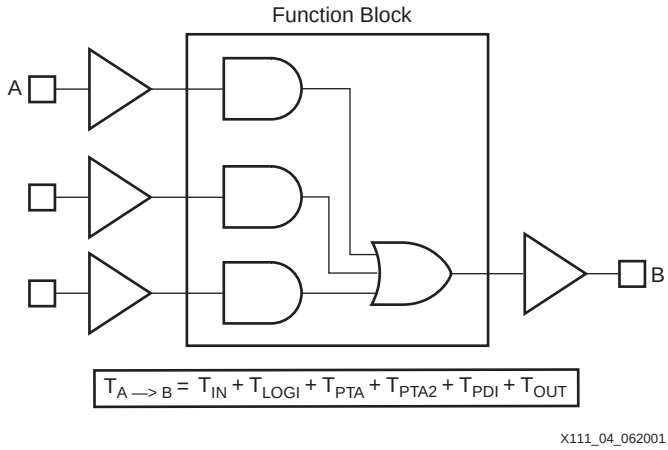


Figure 4: **T_{PD} with Initial Cascaded P-Term from Two Levels**

Figure 5 shows the results of supplementing single pass logic with an additional pass through another macrocell. In this case, there is a single pass through the input and output buffers, two passes through the macrocell logic, and a single pass through the feedback path.

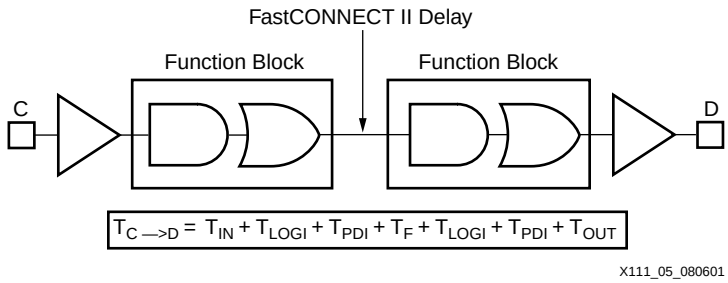
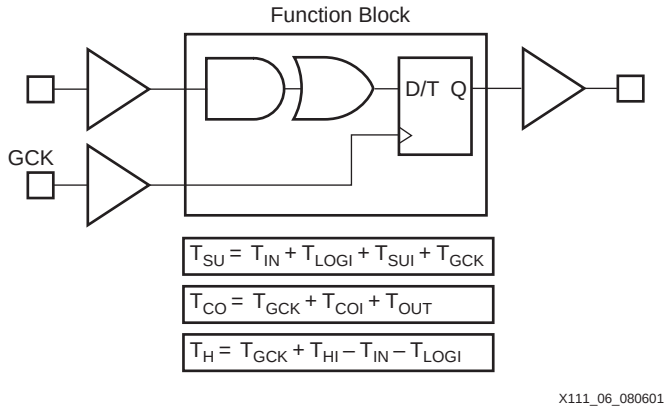


Figure 5: **T_{PD} with Multiple Pass Logic**

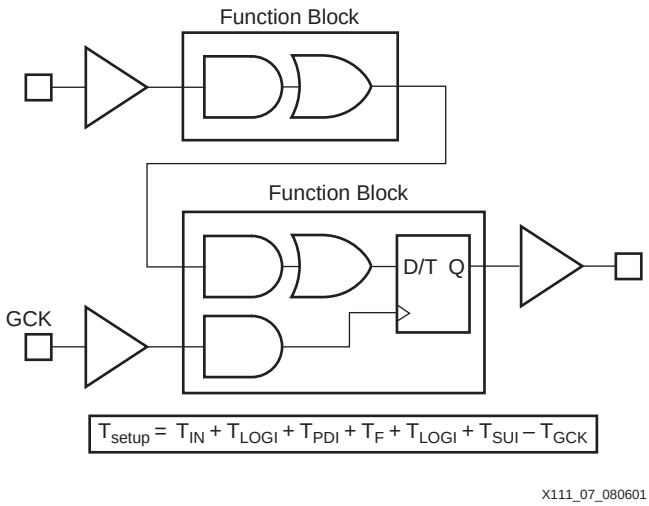
Figure 6 shows the situation for a simple flip-flop clocked by a global clock signal (GCK). The expressions for T_{CO}, T_H, and T_{SU} in Table 2 are valid for this arrangement.



Note: Flip-flop clock-enable not shown

Figure 6: **Simple Flip-Flop Path**

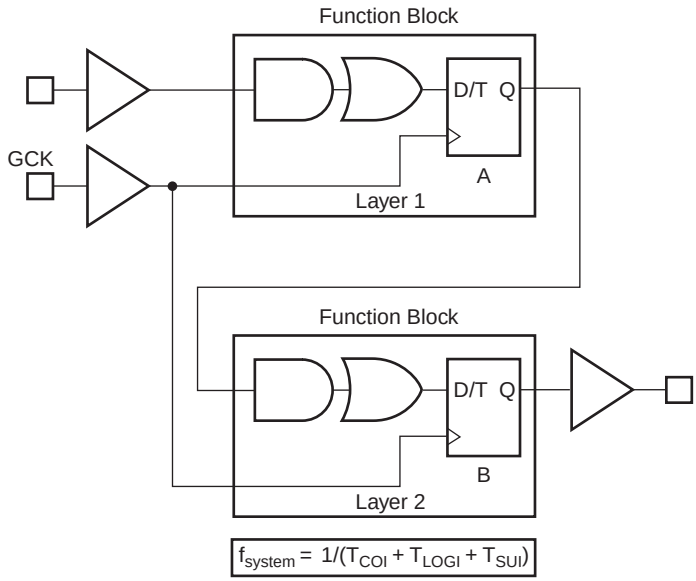
Figure 7 shows the addition of another layer of macrocell logic into the situation described in Figure 6. The T_{CO} and T_H expressions remain the same, but the T_{SU} expression is increased by another $T_{LOGI} + T_{PDI} + T_F$.



Note: Global clock, T_{CO} and T_H are unchanged; EC not shown

Figure 7: **Flip-Flop with Two-Pass Logic**

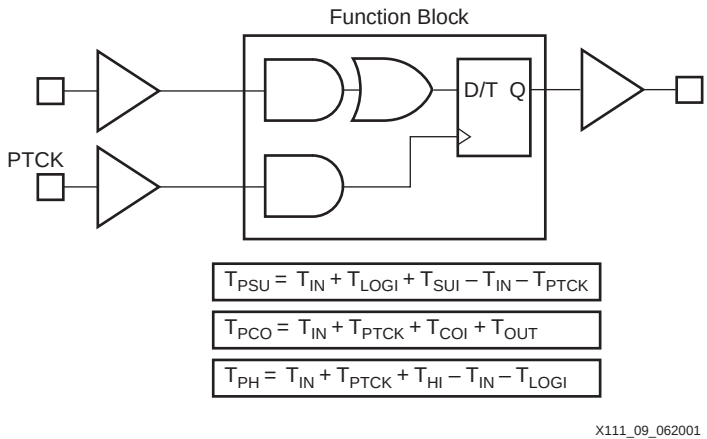
Figure 8 shows two flip-flops connected by a single level of logic, clocked by a global clock. The T_{SU} and T_H for flip-flop A are identical to that of Figure 6.



Note: EC not shown

Figure 8: **Multiple Flip-Flops with Single Level Logic**

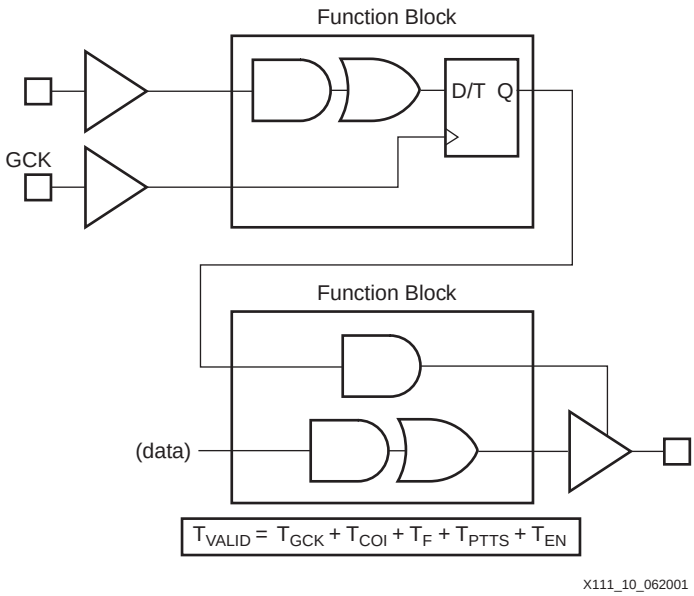
Figure 9 shows a single flip-flop with a product term clock. This arrangement differs from Figure 6 only in that the clock input comes from a product term clock. The entry for T_{PCO} in Table 2 reflects this variation. The timing for T_{PSU} and T_{PH} is calculated using the product term clock timing parameters



Note: EC not shown

Figure 9: **Single Flip-Flop with Product Term Clock**

Figure 10 shows the timing for driving valid data onto a bus with respect to a rising clock edge, a common configuration that occurs in high-speed buses. This is sometimes called T_{VALID}.



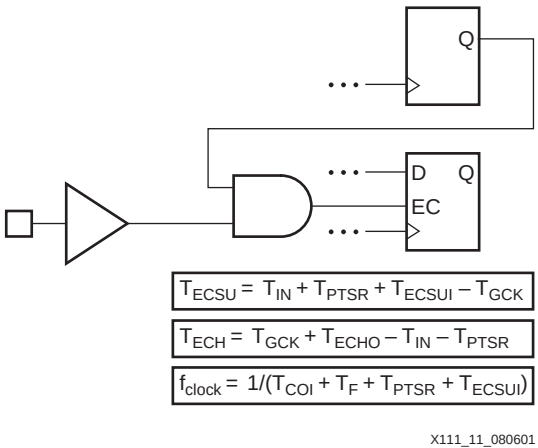
Note: EC not shown

Figure 10: **Flip-Flop Controlled Output Enable**

Figure 6 through Figure 10 do not use the flip-flop clock enable.

Clock Enable (EC) is basically logic inserted before the flip-flop D input. Thus, EC has both setup (T_{ECSU}) and hold (T_{ECH}) time requirements.

Figure 11 shows how EC, which is driven by a product term, impacts f_{MAX}. Any additional feedback delays are added to the T_{setup} and/or f_{clock} calculations, which may impact system clock frequency.



Note: Product term allocator delays (T_{PTA}) and low power logic delays (T_{LOGILP}) do not apply to Clock Enable timing calculations.

Figure 11: **Flip-Flop with Clock Enable**

Low Power Mode

The power consumption of each macrocell in a CPLD device is programmable.The standard (default) setting consumes more power and produces shorter propagation delay. The low-power setting reduces power consumption for less speed-critical paths.

When a macrocell is operating in low power mode, substitute the delay term T_{LOGILP} in all timing calculations where T_{LOGI} normally appears.

Conclusion

This set of examples is sufficient to describe a large number of design configurations, and other examples can easily be derived from the timing model. For manual calculations, other timing delays such as T_{SLEW} and T_{LOGILP} are easily added to the overall timing as required.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
08/20/01	1.0	Initial Xilinx release.