XC4000E Electrical Specifications

Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

Advance: Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or device families. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on preliminary characterization. Further changes are not expected.

Unmarked: Specifications not identified as either Advance or Preliminary are to be considered Final.

Except for pin-to-pin input and output parameters, the a.c. parameter delay specifications included in this document are derived from measuring internal test patterns. All specifications are representative of worst-case supply voltage and junction temperature conditions.

All specifications subject to change without notice.

XC4000E DC Characteristics

Absolute Maximum Ratings

Symbol	Description		Value	Units
V_{CC}	Supply voltage relative to GND		-0.5 to +7.0	V
V_{IN}	Input voltage relative to GND (Note 1)		-0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output (Note 1)		-0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)		-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in. = 1.5 mm)		+260	°C
T_J	Junction Temperature	Ceramic packages	+150	°C
		Plastic packages	+125	°C

Note 1: Maximum DC excursion above V_{cc} or below Ground must be limited to either 0.5 V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to -2.0 V or overshoot to V_{CC} + 2.0 V, provided this over or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA.

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{CC}	Supply voltage relative to GND, T_J = -0 °C to +85°C	Commercial	4.75	5.25	V
	Supply voltage relative to GND, T_J = -40°C to +100°C	Industrial	4.5	5.5	V
	Supply voltage relative to GND, T_C = -55°C to +125°C	Military	4.5	5.5	V
V_{IH}	High-Level Input Voltage	TTL inputs	2.0	V_{CC}	V
		CMOS inputs	70%	100%	V_{CC}
V_{IL}	Low-Level Input Voltage	TTL inputs	0	0.8	V
		CMOS inputs	0	20%	V_{CC}
T_{IN}	Input signal transition time			250	ns

Notes: At junction temperatures above those listed above, all delay parameters increase by 0.35% per °C.
Input and output measurement thresholds for TTL are 1.5 V and for CMOS are 2.5 V.

DC Characteristics Over Operating Conditions

Symbol	Description		Min	Max	Units
V_{OH}	High-level output voltage @ I_{OH} = -4.0mA, V_{CC} min	TTL outputs	2.4		V
	High-level output voltage @ I_{OH} = -1.0mA, V_{CC} min	CMOS outputs	V_{CC}-0.5		V
V_{OL}	Low-level output voltage @ I_{OL} = 12.0mA, V_{CC} min (Note 1)	TTL outputs		0.4	V
		CMOS outputs		0.4	V
I_{CCO}	Quiescent FPGA supply current (Note 2)	Commercial		3.0	mA
		Industrial		6.0	mA
		Military		6.0	mA
I_L	Input or output leakage current		-10	+10	µA
C_{IN}	Input capacitance (sample tested)	PQFP and MQFP packages		10	pF
		Other packages		16	pF
I_{RIN}*	Pad pull-up (when selected) @ V_{IN} = 0V (sample tested)		-0.02	-0.25	mA
I_{RLL}*	Horizontal Longline pull-up (when selected) @ logic Low		0.2	2.5	mA

Notes: With 50% of the outputs simultaneously sinking 12mA, up to a maximum of 64 pins.
With no output current loads, no active input or Longline pull-up resistors, all package pins at Vcc or GND, and the FPGA configured with a Development system Tie option.
*Characterized Only.

XC4000E Switching Characteristics

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

When fewer vertical clock lines are connected, the clock distribution is faster; when multiple clock lines per column are driven from the same global clock, the delay is longer. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation net list. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

Global Buffer Switching Characteristic Guidelines

		Speed Grade	-4	-3	-2	-1	
Description	**Symbol**	**Device**	**Max**	**Max**	**Max**	**Max**	**Units**
From pad through Primary buffer, to any clock K	T_{PG}	XC4003E	7.0	4.7	4.0	3.5	ns
		XC4005E	7.0	4.7	4.3	3.8	ns
		XC4006E	7.5	5.3	5.2	4.6	ns
		XC4008E	8.0	6.1	5.2	4.6	ns
		XC4010E	11.0	6.3	5.4	4.8	ns
		XC4013E	11.5	6.8	5.8	5.2	ns
		XC4020E	12.0	7.0	6.4	6.0	ns
		XC4025E	12.5	7.2	6.9	–	ns
From pad through Secondary buffer, to any clock K	T_{SG}	XC4003E	7.5	5.2	4.4	4.0	ns
		XC4005E	7.5	5.2	4.7	4.3	ns
		XC4006E	8.0	5.8	5.6	5.1	ns
		XC4008E	8.5	6.6	5.6	5.1	ns
		XC4010E	11.5	6.8	5.8	5.3	ns
		XC4013E	12.0	7.3	6.2	5.7	ns
		XC4020E	12.5	7.5	6.7	6.5	ns
		XC4025E	13.0	7.7	7.2	–	ns

Horizontal Longline Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation net list. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000E devices unless otherwise noted. The following guidelines reflect worst-case values over the recommended operating conditions.

		Speed Grade	-4	-3	-2	-1	
Description	**Symbol**	**Device**	**Max**	**Max**	**Max**	**Max**	**Units**
TBUF driving a Horizontal Longline (LL):							
I going High or Low to LL going High or Low, while T is Low. Buffer is constantly active. (Note1)	T_{IO1}	XC4003E	5.0	4.2	3.4	2.9	ns
		XC4005E	5.0	5.0	4.0	3.4	ns
		XC4006E	6.0	5.9	4.7	4.0	ns
		XC4008E	7.0	6.3	5.0	4.3	ns
		XC4010E	8.0	6.4	5.1	4.4	ns
		XC4013E	9.0	7.2	5.7	4.9	ns
		XC4020E	10.0	8.2	7.3	5.6	ns
		XC4025E	11.0	9.1	7.3	–	ns
I going Low to LL going from resistive pull-up High to active Low. TBUF configured as open-drain. (Note1)	T_{IO2}	XC4003E	5.0	4.2	3.6	3.1	ns
		XC4005E	6.0	5.3	4.5	3.8	ns
		XC4006E	7.8	6.4	5.4	4.6	ns
		XC4008E	8.1	6.8	5.8	4.9	ns
		XC4010E	10.5	6.9	5.9	5.0	ns
		XC4013E	11.0	7.7	6.5	5.5	ns
		XC4020E	12.0	8.7	8.7	7.4	ns
		XC4025E	12.0	9.6	9.6	–	ns
T going Low to LL going from resistive pull-up or floating High to active Low. TBUF configured as open-drain or active buffer with I = Low. (Note1)	T_{ON}	XC4003E	5.5	4.6	3.9	3.5	ns
		XC4005E	7.0	6.0	5.7	4.7	ns
		XC4006E	7.5	6.7	5.7	4.9	ns
		XC4008E	8.0	7.1	6.0	5.2	ns
		XC4010E	8.5	7.3	6.2	5.4	ns
		XC4013E	8.7	7.5	7.0	6.2	ns
		XC4020E	11.0	8.4	7.1	6.3	ns
		XC4025E	11.0	8.4	7.1	–	ns
T going High to TBUF going inactive, not driving LL	T_{OFF}	All devices	1.8	1.5	1.3	1.1	ns
T going High to LL going from Low to High, pulled up by a single resistor. (Note 1)	T_{PUS}	XC4003E	20.0	14.0	14.0	12.0	ns
		XC4005E	23.0	16.0	16.0	14.0	ns
		XC4006E	25.0	18.0	18.0	16.0	ns
		XC4008E	27.0	20.0	20.0	16.0	ns
		XC4010E	29.0	22.0	22.0	18.0	ns
		XC4013E	32.0	26.0	26.0	21.0	ns
		XC4020E	35.0	32.5	32.5	26.0	ns
		XC4025E	42.0	39.1	39.1	–	ns
T going High to LL going from Low to High, pulled up by two resistors. (Note1)	T_{PUF}	XC4003E	9.0	7.0	6.0	5.4	ns
		XC4005E	10.0	8.0	6.8	5.8	ns
		XC4006E	11.5	9.0	7.7	6.5	ns
		XC4008E	12.5	10.0	8.5	7.5	ns
		XC4010E	13.5	11.0	9.4	8.0	ns
		XC4013E	15.0	13.0	11.7	9.4	ns
		XC4020E	16.0	14.8	14.8	10.5	ns
		XC4025E	18.0	16.5	16.5	–	ns

Note 1: These values include a minimum load. Use the static timing analyzer to determine the delay for each destination.

Wide Decoder Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation net list. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000E devices unless otherwise noted. The following guidelines reflect worst-case values over the recommended operating conditions.

		Speed Grade	-4	-3	-2	-1	
Description	**Symbol**	**Device**	**Max**	**Max**	**Max**	**Max**	**Units**
Full length, both pull-ups, inputs from IOB I-pins	T_{WAF}	XC4003E	9.2	5.0	5.0	4.3	ns
		XC4005E	9.5	6.0	6.0	5.1	ns
		XC4006E	12.0	7.0	7.0	6.0	ns
		XC4008E	12.5	8.0	8.0	6.5	ns
		XC4010E	15.0	9.0	9.0	7.5	ns
		XC4013E	16.0	11.0	11.0	8.6	ns
		XC4020E	17.0	13.9	13.9	10.1	ns
		XC4025E	18.0	16.9	16.9	–	ns
Full length, both pull-ups, inputs from internal logic	T_{WAFL}	XC4003E	12.0	7.0	7.0	5.5	ns
		XC4005E	12.5	8.0	8.0	6.4	ns
		XC4006E	14.0	9.0	9.0	7.0	ns
		XC4008E	16.0	10.0	10.0	7.5	ns
		XC4010E	18.0	11.0	11.0	8.5	ns
		XC4013E	19.0	13.0	13.0	10.0	ns
		XC4020E	20.0	15.5	15.5	11.8	ns
		XC4025E	21.0	18.9	18.9	–	ns
Half length, one pull-up, inputs from IOB I-pins	T_{WAO}	XC4003E	10.5	6.0	6.0	5.1	ns
		XC4005E	10.5	7.0	7.0	6.0	ns
		XC4006E	13.5	8.0	8.0	6.5	ns
		XC4008E	14.0	9.0	9.0	7.0	ns
		XC4010E	16.0	10.0	10.0	7.5	ns
		XC4013E	17.0	12.0	12.0	10.0	ns
		XC4020E	18.0	15.0	15.0	11.8	ns
		XC4025E	19.0	17.6	17.6	–	ns
Half length, one pull-up, inputs from internal logic	T_{WAOL}	XC4003E	12.0	8.0	8.0	6.0	ns
		XC4005E	12.5	9.0	9.0	7.0	ns
		XC4006E	14.0	10.0	10.0	7.6	ns
		XC4008E	16.0	11.0	11.0	8.4	ns
		XC4010E	18.0	12.0	12.0	9.2	ns
		XC4013E	19.0	14.0	14.0	10.8	ns
		XC4020E	20.0	16.8	16.8	12.6	ns
		XC4025E	21.0	19.6	19.6	–	ns

Note 1: These delays are specified from the decoder input to the decoder output.
Note 2: Fewer than the specified number of pullup resistors can be used, if desired. Using fewer pullups reduces power consumption but increases delays. Use the static timing analyzer to determine delays if fewer pullups are used.

XC4000E CLB Characteristics Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation net list. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000E devices unless otherwise noted

CLB Switching Characteristics Guidelines

Speed Grade		-4		-3		-2		-1		Units
Description	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
Combinatorial Delays										
F/G inputs to X/Y outputs	T_{ILO}		2.7		2.0		1.6		1.3	ns
F/G inputs via H to X/Y outputs	T_{IHO}		4.7		4.3		2.7		2.2	ns
C inputs via SR through H to X/Y outputs	T_{HH0O}		4.1		3.3		2.4		1.9	ns
C inputs via H to X/Y outputs	T_{HH1O}		3.7		3.6		2.2		1.6	ns
C inputs via DIN through H to X/Y outputs	T_{HH2O}		4.5		3.6		2.6		1.9	ns
CLB Fast Carry Logic										
Operand inputs (F1, F2, G1, G4) to COUT	T_{OPCY}		3.2		2.6		2.1		1.7	ns
Add/Subtract input (F3) to COUT	T_{ASCY}		5.5		4.4		3.7		2.5	ns
Initialization inputs (F1, F3) to COUT	T_{INCY}		1.7		1.7		1.4		1.2	ns
CIN through function generators to X/Y outputs	T_{SUM}		3.8		3.3		2.6		1.8	ns
CIN to COUT, bypass function generators	T_{BYP}		1.0		0.7		0.6		0.5	ns
Sequential Delays										
Clock K to outputs Q	T_{CKO}		3.7		2.8		2.8		1.9	ns
Setup Time before Clock K										
F/G inputs	T_{ICK}	4.0		3.0		2.4		1.8		ns
F/G inputs via H	T_{IHCK}	6.1		4.6		3.9		2.8		ns
C inputs via H0 through H	T_{HH0CK}	4.5		3.6		3.5		2.4		ns
C inputs via H1 through H	T_{HH1CK}	5.0		4.1		3.3		2.1		ns
C inputs via H2 through H	T_{HH2CK}	4.8		3.8		3.7		2.5		ns
C inputs via DIN	T_{DICK}	3.0		2.4		2.0		1.0		ns
C inputs via EC	T_{ECCK}	4.0		3.0		2.6		2.0		ns
C inputs via S/R, going Low (inactive)	T_{RCK}	4.2		4.0		4.0		1.5		ns
C_{IN} input via F/G	T_{CCK}	2.5		2.1						ns
C_{IN} input via F/G and H	T_{CHCK}	4.2		3.5						ns

XC4000E CLB Characteristics Guidelines (Continued)

Speed Grade		-4		-3		-2		-1		Units
Description	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
Hold Time after Clock K										
F/G inputs	T_{CKI}	0		0		0		0		ns
F/G inputs via H	T_{CKIH}	0		0		0		0		ns
C inputs via H0 through H	T_{CKHH0}	0		0		0		0		ns
C inputs via H1 through H	T_{CKHH1}	0		0		0		0		ns
C inputs via H2 through H	T_{CKHH2}	0		0		0		0		ns
C inputs via DIN	T_{CKDI}	0		0		0		0		ns
C inputs via EC	T_{CKEC}	0		0		0		0		ns
C inputs via SR, going Low (inactive)	T_{CKR}	0		0		0		0		ns
Clock										
Clock High time	T_{CH}	4.5		4.0		4.0		3.0		ns
Clock Low time	T_{CL}	4.5		4.0		4.0		3.0		ns
Set/Reset Direct										
Width (High)	T_{RPW}	5.5		4.0		4.0		3.0		ns
Delay from C inputs via S/R, going High to Q	T_{RIO}		6.5		4.0		4.0		3.0	ns
Master Set/Reset (Note 1)										
Width (High or Low)	T_{MRW}	13.0		11.5		11.5		10.0		ns
Delay from Global Set/Reset net to Q	T_{MRQ}		23.0		18.7		17.4		15.0	ns
Global Set/Reset inactive to first active clock K edge	T_{MRK}									
Toggle Frequency (Note 2)	F_{TOG}		111		125		125		166	MHz

Note 1: Timing is based on the XC4005E. For other devices see the static timing analyzer.
Note 2: Export Control Max. flip-flop toggle rate.

CLB Edge-Triggered (Synchronous) RAM Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation net list. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000E devices unless otherwise noted.

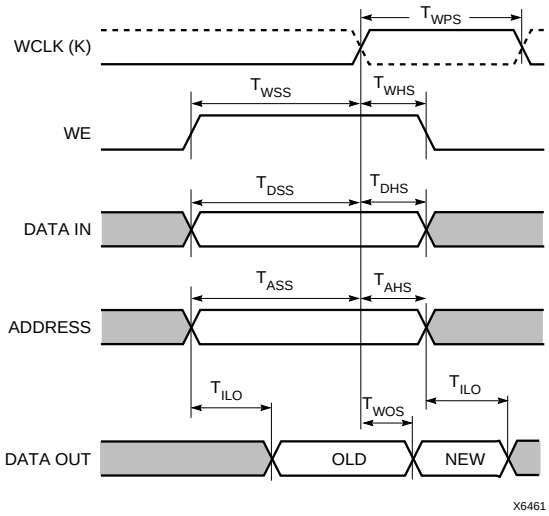
Single Port RAM	Speed Grade		-4		-3		-2		-1		Units
	Size	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	
Write Operation											
Address write cycle time (clock K period)	16x2 32x1	T_{WCS} T_{WCTS}	15.0 15.0		14.4 14.4		11.6 11.6		8.0 8.0		ns ns
Clock K pulse width (active edge)	16x2 32x1	T_{WPS} T_{WPTS}	7.5 7.5	1 ms 1 ms	7.2 7.2	1 ms 1 ms	5.8 5.8	1 ms 1 ms	4.0 4.0		ns ns
Address setup time before clock K	16x2 32x1	T_{ASS} T_{ASTS}	2.8 2.8		2.4 2.4		2.0 2.0		1.5 1.5		ns ns
Address hold time after clock K	16x2 32x1	T_{AHS} T_{AHTS}	0 0		0 0		0 0		0 0		ns ns
DIN setup time before clock K	16x2 32x1	T_{DSS} T_{DSTS}	3.5 2.5		3.2 1.9		2.7 1.7		1.5 1.5		ns ns
DIN hold time after clock K	16x2 32x1	T_{DHS} T_{DHTS}	0 0		0 0		0 0		0 0		ns ns
WE setup time before clock K	16x2 32x1	T_{WSS} T_{WSTS}	2.2 2.2		2.0 2.0		1.6 1.6		1.5 1.5		ns ns
WE hold time after clock K	16x2 32x1	T_{WHS} T_{WHTS}	0 0		0 0		0 0		0 0		ns ns
Data valid after clock K	16x2 32x1	T_{WOS} T_{WOTS}		10.3 11.6		8.8 10.3		7.9 9.3		6.5 7.0	ns ns

Note 1: Timing for the 16x1 RAM option is identical to 16x2 RAM timing.
Note 2: Applicable Read timing specifications are identical to Level-Sensitive Read timing.

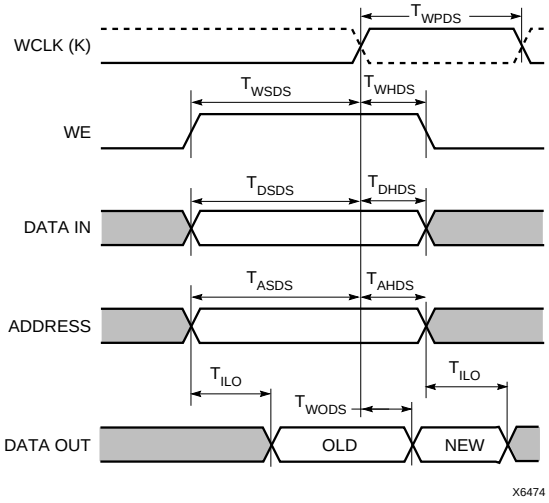
Dual-Port RAM	Speed Grade		-4		-3		-2		-1		Units
	Size	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	
Write Operation											
Address write cycle time (clock K period)	16x1	T_{WCDS}	15.0		14.4		11.6		8.0		ns
Clock K pulse width (active edge)	16x1	T_{WPDS}	7.5	1 ms	7.2	1 ms	5.8	1 ms	4.0		ns
Address setup time before clock K	16x1	T_{ASDS}	2.8		2.5		2.1		1.5		ns
Address hold time after clock K	16x1	T_{AHDS}	0		0		0		0		ns
DIN setup time before clock K	16x1	T_{DSDS}	2.2		2.5		1.6		1.5		ns
DIN hold time after clock K	16x1	T_{DHDS}	0		0		0		0		ns
WE setup time before clock K	16x1	T_{WSDS}	2.2		1.8		1.6		1.5		ns
WE hold time after clock K	16x1	T_{WHDS}	0.3		0		0		0		ns
Data valid after clock K	16x1	T_{WODS}		10.0		7.8		7.0		6.5	ns

Note: Applicable Read timing specifications are identical to Level-Sensitive Read timing

CLB RAM Synchronous (Edge-Triggered) Write Timing Waveforms



Single Port



Dual Port

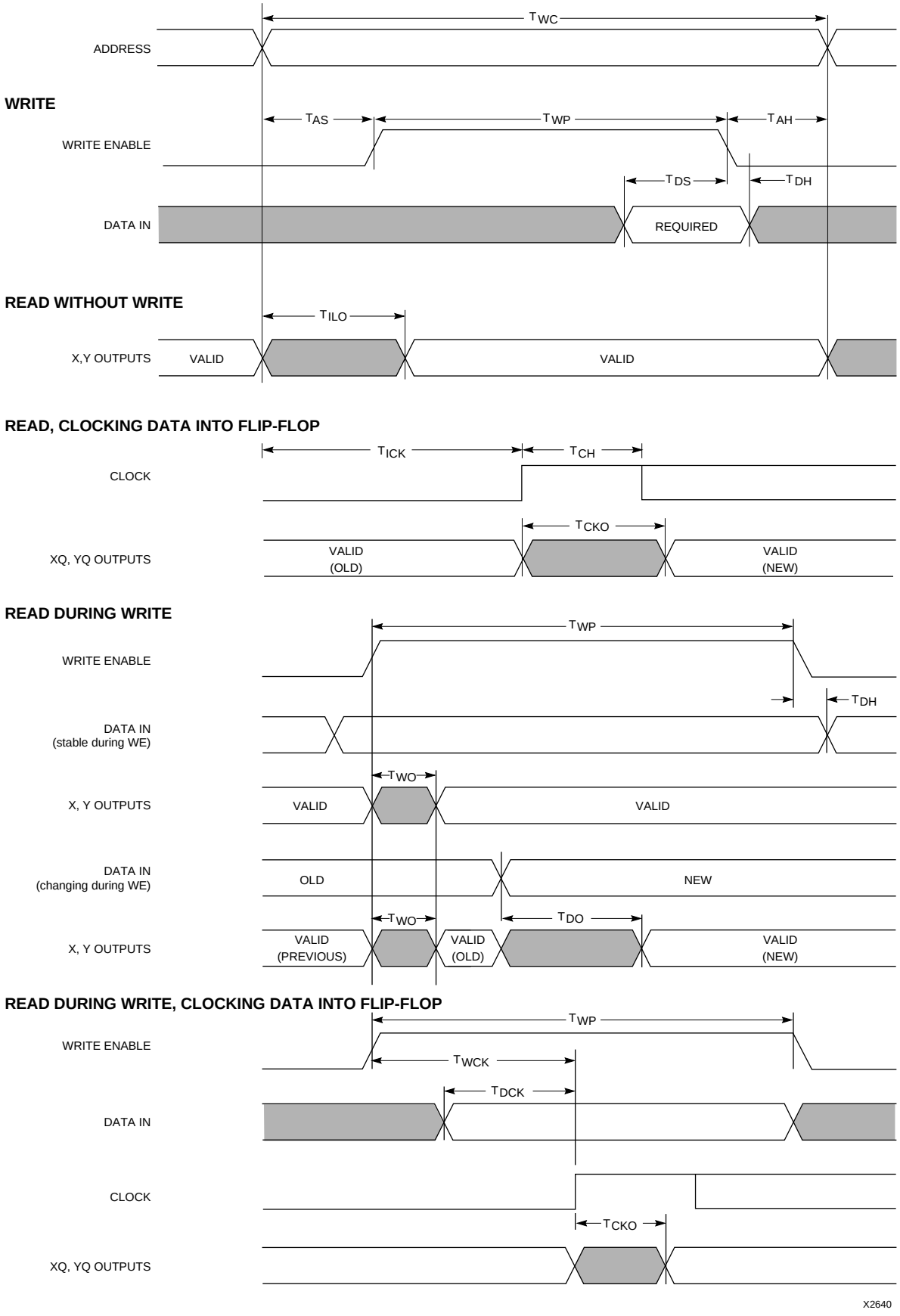
CLB Level-Sensitive RAM Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation net list. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000E devices unless otherwise noted.

Description	Size	Symbol	-4 Min	-4 Max	-3 Min	-3 Max	-2 Min	-2 Max	-1 Min	-1 Max	Units
Write Operation											
Address write cycle time	16x2 32x1	T_{WC} T_{WCT}	8.0 8.0		8.0 8.0		8.0 8.0		8.0 8.0		ns ns
Write Enable pulse width (High)	16x2 32x1	T_{WP} T_{WPT}	4.0 4.0		4.0 4.0		4.0 4.0		4.0 4.0		ns ns
Address setup time before WE	16x2 32x1	T_{AS} T_{AST}	2.0 2.0		2.0 2.0		2.0 2.0		2.0 2.0		ns ns
Address hold time after end of WE	16x2 32x1	T_{AH} T_{AHT}	2.5 2.0		2.0 2.0		2.0 2.0		2.0 2.0		ns ns
DIN setup time before end of WE	16x2 32x1	T_{DS} T_{DST}	4.0 5.0		2.2 2.2		0.8 0.8		0.8 0.8		ns ns
DIN hold time after end of WE	16x2 32x1	T_{DH} T_{DHT}	2.0 2.0		2.0 2.0		2.0 2.0		2.0 2.0		ns ns
Read Operation											
Address read cycle time	16x2 32x1	T_{RC} T_{RCT}	4.5 6.5		3.1 5.5		2.6 3.8		2.6 3.8		ns ns
Data valid after address change (no Write Enable)	16x2 32x1	T_{ILO} T_{IHO}		2.7 4.7		1.8 3.2		1.6 2.7		1.6 2.7	ns ns
Read Operation, Clocking Data into Flip-Flop											
Address setup time before clock K	16x2 32x1	T_{ICK} T_{IHCK}	4.0 6.1		3.0 4.6		2.4 3.9		2.4 3.9		ns ns
Read During Write											
Data valid after WE goes active (DIN stable before WE)	16x2 32x1	T_{WO} T_{WOT}		10.0 12.0		6.0 7.3		4.9 5.6		4.9 5.6	ns ns
Data valid after DIN (DIN changes during WE)	16x2 32x1	T_{DO} T_{DOT}		9.0 11.0		6.6 7.6		5.8 6.2		5.8 6.2	ns ns
Read During Write, Clocking Data into Flip-Flop											
WE setup time before clock K	16x2 32x1	T_{WCK} T_{WCKT}	8.0 9.6		6.0 6.8		5.1 5.8		5.1 5.8		ns ns
Data setup time before clock K	16x2 32x1	T_{DCK} T_{DCKT}	7.0 8.0		5.2 6.2		4.4 5.3		4.4 5.3		ns ns

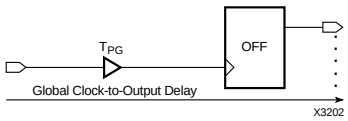
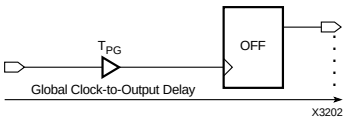
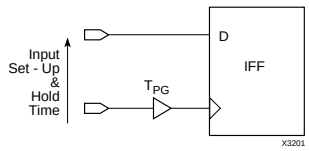
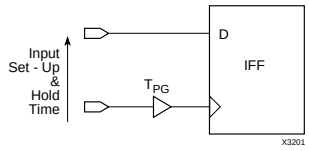
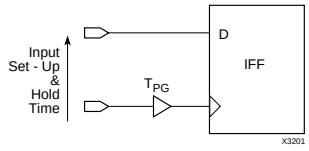
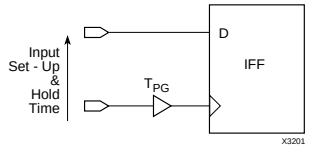
Note 1: Timing for the 16x1 RAM option is identical to 16x2 RAM timing.

CLB Level-Sensitive RAM Timing Waveforms



XC4000E Guaranteed Input and Output Parameters (Pin-to-Pin, TTL I/O)

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation net list. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values apply to all XC4000E devices unless otherwise noted.

Description	Symbol	Speed Grade: Device	-4	-3	-2	-1	Units
Global Clock to Output (fast) using OFF 	T_{ICKOF} (Max)	XC4003E	12.5	10.2	8.7	5.8	ns
		XC4005E	14.0	10.7	9.1	6.2	ns
		XC4006E	14.5	10.7	9.1	6.4	ns
		XC4008E	15.0	10.8	9.2	6.6	ns
		XC4010E	16.0	10.9	9.3	6.8	ns
		XC4013E	16.5	11.0	9.4	7.2	ns
		XC4020E	17.0	11.0	10.2	7.4	ns
		XC4025E	17.0	12.6	10.8	–	ns
Global Clock to Output (slew-limited) using OFF 	T_{ICKO} (Max)	XC4003E	16.5	14.0	11.5	7.8	ns
		XC4005E	18.0	14.7	12.0	8.2	ns
		XC4006E	18.5	14.7	12.0	8.4	ns
		XC4008E	19.0	14.8	12.1	8.6	ns
		XC4010E	20.0	14.9	12.2	8.8	ns
		XC4013E	20.5	15.0	12.8	9.2	ns
		XC4020E	21.0	15.1	12.8	9.4	ns
		XC4025E	21.0	15.3	13.0	–	ns
Input Setup Time, using IFF (no delay) 	T_{PSUF} (Min)	XC4003E	2.5	2.3	2.3	1.5	ns
		XC4005E	2.0	1.2	1.2	0.8	ns
		XC4006E	1.9	1.0	1.0	0.6	ns
		XC4008E	1.4	0.6	0.6	0.2	ns
		XC4010E	1.0	0.2	0.2	0	ns
		XC4013E	0.5	0	0	0	ns
		XC4020E	0	0	0	0	ns
		XC4025E	0	0	0	–	ns
Input Hold Time, using IFF (no delay) 	T_{PHF} (Min)	XC4003E	4.0	4.0	4.0	1.5	ns
		XC4005E	4.6	4.5	4.5	2.0	ns
		XC4006E	5.0	4.7	4.7	2.0	ns
		XC4008E	6.0	5.1	5.1	2.5	ns
		XC4010E	6.0	5.5	5.5	2.5	ns
		XC4013E	7.0	6.5	5.5	3.0	ns
		XC4020E	7.5	6.7	5.7	3.5	ns
		XC4025E	8.0	7.0	5.9	–	ns
Input Setup Time, using IFF (with delay) 	T_{PSU} (Min)	XC4003E	8.5	7.0	6.0	5.0	ns
		XC4005E	8.5	7.0	6.0	5.0	ns
		XC4006E	8.5	7.0	6.0	5.0	ns
		XC4008E	8.5	7.0	6.0	5.0	ns
		XC4010E	8.5	7.0	6.0	5.0	ns
		XC4013E	8.5	7.0	6.0	5.0	ns
		XC4020E	9.5	7.0	6.8	5.0	ns
		XC4025E	9.5	7.6	6.8	–	ns
Input Hold Time, using IFF (with delay) 	T_{PH} (Min)	XC4003E	0	0	0	0	ns
		XC4005E	0	0	0	0	ns
		XC4006E	0	0	0	0	ns
		XC4008E	0	0	0	0	ns
		XC4010E	0	0	0	0	ns
		XC4013E	0	0	0	0	ns
		XC4020E	0	0	0	0	ns
		XC4025E	0	0	0	–	ns

OFF = Output Flip-Flop, IFF = Input Flip-Flop or Latch

XC4000E IOB Input Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation net list. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values apply to all XC4000E devices unless otherwise noted.

	Speed Grade		-4		-3		-2		-1		Units
Description	**Symbol**	**Device**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
Propagation Delays (TTL Inputs)											
Pad to I1, I2											
Pad to I1, I2 via transparent	T_{PID}	All devices		3.0		2.5		2.0		1.4	ns
latch, no delay											
with delay	T_{PLI}	All devices		4.8		3.6		3.6		2.8	ns
	T_{PDLI}	XC4003E		10.4		9.3		6.9		6.4	ns
		XC4005E		10.8		9.6		7.4		6.5	ns
		XC4006E		10.8		10.2		8.1		6.9	ns
		XC4008E		10.8		10.6		8.2		7.0	ns
		XC4010E		11.0		10.8		8.3		7.3	ns
		XC4013E		11.4		11.2		9.8		8.4	ns
		XC4020E		13.8		12.4		11.5		9.0	ns
		XC4025E		13.8		13.7		12.4		–	ns
Propagation Delays (CMOS Inputs)											
Pad to I1, I2	T_{PIDC}	All devices		5.5		4.1		3.7		1.9	ns
Pad to I1, I2 via transparent											
latch, no delay	T_{PLIC}	All devices		8.8		6.8		6.2		3.3	ns
with delay	T_{PDLIC}	XC4003E		16.5		12.4		11.0		6.9	ns
		XC4005E		16.5		13.2		11.9		7.0	ns
		XC4006E		16.8		13.4		12.1		7.4	ns
		XC4008E		17.3		13.8		12.4		7.4	ns
		XC4010E		17.5		14.0		12.6		7.8	ns
		XC4013E		18.0		14.4		13.0		9.0	ns
		XC4020E		20.8		15.6		14.0		9.5	ns
		XC4025E		20.8		15.6		14.0		–	ns
Propagation Delays											
Clock (IK) to I1, I2 (flip-flop)	T_{IKRI}	All devices		5.6		2.8		2.8		2.7	ns
Clock (IK) to I1, I2											
(latch enable, active Low)	T_{IKLI}	All devices		6.2		4.0		3.9		3.2	ns
Hold Times (Note 1)											
Pad to Clock (IK), no delay	T_{IKPI}	All devices	0		0		0		0		ns
with delay	T_{IKPID}	All devices	0		0		0		0		ns
Clock Enable (EC) to Clock (IK),											
no delay	T_{IKEC}	All devices	1.5		1.5		0.9		0		ns
with delay	T_{IKECD}	All devices	0		0		0		0		ns

Note 1: Input pad setup and hold times are specified with respect to the internal clock (IK). For setup and hold times with respect to the clock input pin, see the pin-to-pin parameters in the Guaranteed Input and Output Parameters table.

Note 2: Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

XC4000E IOB Input Switching Characteristic Guidelines (Continued)

Description	Speed Grade Symbol	Device	-4 Min	-4 Max	-3 Min	-3 Max	-2 Min	-2 Max	-1 Min	-1 Max	Units
Setup Times (TTL Inputs)											
Pad to Clock (IK), no delay	T_{PICK}	All devices	4.0		2.6		2.0		1.5		ns
with delay	T_{PICKD}	XC4003E	10.9		8.2		6.0		4.8		ns
		XC4005E	10.9		8.7		6.1		5.1		ns
		XC4006E	10.9		9.2		6.2		5.8		ns
		XC4008E	11.1		9.6		6.3		5.8		ns
		XC4010E	11.3		9.8		6.4		6.0		ns
		XC4013E	11.8		10.2		7.9		7.6		ns
		XC4020E	14.0		11.4		9.4		8.2		ns
		XC4025E	14.0		11.4		10.0		–		ns
Setup Time (CMOS Inputs)											
Pad to Clock (IK), no delay	T_{PICKC}	All devices	6.0		3.3		2.4		2.4		ns
with delay	T_{PICKDC}	XC4003E	12.0		8.8		6.9		5.3		ns
		XC4005E	12.0		9.7		8.0		5.6		ns
		XC4006E	12.3		9.9		8.1		6.3		ns
		XC4008E	12.8		10.3		8.2		6.3		ns
		XC4010E	13.0		10.5		8.3		6.5		ns
		XC4013E	13.5		10.9		10.0		7.9		ns
		XC4020E	16.0		12.1		12.1		8.1		ns
		XC4025E	16.0		12.1		12.1		–		ns
(TTL or CMOS)											
Clock Enable (EC) to Clock (IK), no delay	T_{ECIK}	All devices	3.5		2.5		2.1		1.5		ns
with delay	T_{ECIKD}	XC4003E	10.4		8.1		4.3		4.3		ns
		XC4005E	10.4		8.5		5.6		5.0		ns
		XC4006E	10.4		9.1		6.7		6.0		ns
		XC4008E	10.4		9.5		6.9		6.0		ns
		XC4010E	10.7		9.7		7.1		6.5		ns
		XC4013E	11.1		10.1		9.0		8.0		ns
		XC4020E	14.0		11.3		10.6		9.0		ns
		XC4025E	14.0		11.3		11.0		–		ns
Global Set/Reset (Note 3)											
Delay from GSR net through Q to I1, I2	T_{RRI}			12.0		7.8		6.8		6.8	ns
GSR width	T_{MRW}		13.0		11.5		11.5		10.0		ns
GSR inactive to first active Clock (IK) edge	T_{MRI}										

Note 1: Input pad setup and hold times are specified with respect to the internal clock (IK). For setup and hold times with respect to the clock input pin, see the pin-to-pin parameters in the Guaranteed Input and Output Parameters table.

Note 2: Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

Note 3: Timing is based on the XC4005E. For other devices see the XACT timing calculator.

XC4000E IOB Output Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation net list. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000E devices unless otherwise noted.

Speed Grade		-4		-3		-2		-1		Units
Description	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
Propagation Delays (TTL Output Levels)										
Clock (OK) to Pad, fast	T_{OKPOF}		7.5		6.5		4.5	3.0		ns
slew-rate limited	T_{OKPOS}		11.5		9.5		7.0	5.0		ns
Output (O) to Pad, fast	T_{OPF}		8.0		5.5		4.8	3.2		ns
slew-rate limited	T_{OPS}		12.0		8.5		7.3	5.2		ns
3-state to Pad hi-Z (slew-rate independent)	T_{TSHZ}		5.0		4.2		3.8	3.0		ns
3-state to Pad active and valid, fast	T_{TSONF}		9.7		8.1		7.3	6.8		ns
slew-rate limited	T_{TSONS}		13.7		11.1		9.8	8.8		ns
Propagation Delays (CMOS Output Levels)										
Clock (OK) to Pad, fast	T_{OKPOFC}		9.5		7.8		7.0		4.0	ns
slew-rate limited	T_{OKPOSC}		13.5		11.6		10.4		7.0	ns
Output (O) to Pad, fast	T_{OPFC}		10.0		9.7		8.7		4.0	ns
slew-rate limited	T_{OPSC}		14.0		13.4		12.1		6.0	ns
3-state to Pad hi-Z (slew-rate independent)	T_{TSHZC}		5.2		4.3		3.9		3.9	ns
3-state to Pad active and valid, fast	T_{TSONFC}		9.1		7.6		6.8		6.8	ns
slew-rate limited	T_{TSONSC}		13.1		11.4		10.2		8.8	ns

Note 1: Output timing is measured at pin threshold, with 50pF external capacitive loads (incl. test fixture). Slew-rate limited output rise/fall times are approximately two times longer than fast output rise/fall times. For the effect of capacitive loads on ground bounce, see the “Additional XC4000 Data” section of the Programmable Logic Data Book.

Note 2: Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

IOB Output Switching Characteristics Guidelines (Continued)

Speed Grade		-4		-3		-2		-1		Units
Description	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
Setup and Hold										
Output (O) to clock (OK) setup time	T_{OOK}	5.0		4.6		3.8		2.3		ns
Output (O) to clock (OK) hold time	T_{OKO}	0		0		0		0		ns
Clock Enable (EC) to clock (OK) setup	T_{ECOK}	4.8		3.5		2.7		2.0		ns
Clock Enable (EC) to clock (OK) hold	T_{OKEC}	1.2		1.2		0.5		0		ns
Clock										
Clock High	T_{CH}	4.5		4.0		4.0			3.0	ns
Clock Low	T_{CL}	4.5		4.0		4.0			3.0	ns
Global Set/Reset (Note 3)										
Delay from GSR net to Pad	T_{RPO}		15.0		11.8		8.7		7.0	ns
GSR width	T_{MRW}	13.0		11.5		11.5				ns
GSR inactive to first active clock (OK) edge	T_{MRO}									

Note 1: Output timing is measured at pin threshold, with 50pF external capacitive loads (incl. test fixture). Slew-rate limited output rise/fall times are approximately two times longer than fast output rise/fall times. For the effect of capacitive loads on ground bounce, see the “Additional XC4000 Data” section of the Programmable Logic Data Book.

Note 2: Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

Note 3: Timing is based on the XC4005E. For other devices see the XACT timing calculator.

XC4000E Boundary Scan (JTAG) Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC4000E devices unless otherwise noted.

Speed Grade		-4		-3		-2		-1		Units
Description	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
Setup Times										
Input (TDI) to clock (TCK) Input (TMS) to clock (TCK)	T_{TDITCK} T_{TMSTCK}	30.0 15.0		30.0 15.0		30.0 15.0		20.0 10.0		ns ns
Hold Times										
Input (TDI) to clock (TCK) Input (TMS) to clock (TCK)	T_{TCKTDI} T_{TCKTMS}	0 0		0 0		0 0		0 0		ns ns
Propagation Delay										
Clock (TCK) to Pad (TDO)	T_{TCKPO}		30.0		30.0		30.0		20.0	ns
Clock										
Clock (TCK) High Clock (TCK) Low	T_{TCKH} T_{TCKL}	5.0 5.0		5.0 5.0		5.0 5.0		4.0 4.0		ns ns
Frequency	F_{MAX}		15.0		15.0		15.0		25.0	MHz

Note 1: Input setup and hold times and clock-to-pad times are specified with respect to external signal pins.
Note 2: Output timing is measured at pin threshold, with 50pF external capacitive loads (incl. test fixture). Slew-rate limited output rise/fall times are approximately two times longer than fast output rise/fall times. For the effect of capacitive loads on ground bounce, see the “Additional XC4000 Data” section of the Programmable Logic Data Book.
Note 3: Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

Revision Control

Version	Nature of Changes
3/30/98 (1.5)	As submitted for the 1999 data book
1/29/99 (1.5)	Updated Switching Characteristics Tables
5/14/99 (1.6)	Replaced Electrical Specification and pinout pages for E, EX, and XL families with separate updates and added URL link on placeholder page for electrical specifications/pinouts for WebLINX users
8/27/99 (1.7)	Included missing IOB Propagation Delay page (6-113)
2/11/00 (1.8)	Altered IOB heads (Acrobat PDF file problem), corrected Dual-port Write Mins for -4 speed grade.