Virtex-E Pin Definitions

Pin Name	Dedicated Pin	Direction	Description
GCK0, GCK1, GCK2, GCK3	Yes	Input	Clock input pins that connect to Global Clock Buffers. These pins become user inputs when not needed for clocks.
M0, M1, M2	Yes	Input	Mode pins are used to specify the configuration mode.
CCLK	Yes	Input or Output	The configuration Clock I/O pin: it is an input for SelectMAP and slave-serial modes, and output in master-serial mode. After configuration, it is input only, logic level = Don't Care.
PROGRAM	Yes	Input	Initiates a configuration sequence when asserted Low.
DONE	Yes	Bidirectional	Indicates that configuration loading is complete, and that the start-up sequence is in progress. The output can be open drain.
INIT	No	Bidirectional (Open-drain)	When Low, indicates that the configuration memory is being cleared. The pin becomes a user I/O after configuration.
BUSY/DOUT	No	Output	In SelectMAP mode, BUSY controls the rate at which configuration data is loaded. The pin becomes a user I/O after configuration unless the SelectMAP port is retained. In bit-serial modes, DOUT provides preamble and configuration data to downstream devices in a daisy-chain. The pin becomes a user I/O after configuration.
D0/DIN, D1, D2, D3, D4, D5, D6, D7	No	Input or Output	In SelectMAP mode, D0-7 are configuration data pins. These pins become user I/Os after configuration unless the SelectMAP port is retained. In bit-serial modes, DIN is the single data input. This pin becomes a user I/O after configuration.
WRITE	No	Input	In SelectMAP mode, the active-low Write Enable signal. The pin becomes a user I/O after configuration unless the SelectMAP port is retained.
CS	No	Input	In SelectMAP mode, the active-low Chip Select signal. The pin becomes a user I/O after configuration unless the SelectMAP port is retained.
TDI, TDO, TMS, TCK	Yes	Mixed	Boundary-scan Test-Access-Port pins, as defined in IEEE1149.1.
DXN, DXP	Yes	N/A	Temperature-sensing diode pins. (Anode: DXP, cathode: DXN)
V_{CCINT}	Yes	Input	Power-supply pins for the internal core logic.
V_{CCO}	Yes	Input	Power-supply pins for the output drivers (subject to banking rules)
V_{REF}	No	Input	Input threshold voltage pins. Become user I/Os when an external threshold voltage is not needed (subject to banking rules).
GND	Yes	Input	Ground

BG560 Ball Grid Array Packages

XCV405E and the XCV812E Virtex-E Extended Memory devices are available in the BG560 BGA package. Pins labeled I0_VREF can be used as either in all parts unless device-dependent as indicated in the footnotes. If the pin is not used as V_{REF}, it can be used as general I/O. Immediately following Table 1, see Table 2 for BG560 package Differential Pair information.

Table 1: **BG560 BGA — XCV405E and XCV812E**

Bank	Pin Description	Pin#
0	GCK3	A17
0	IO	A27
0	IO	B25
0	IO	C28
0	IO	C30
0	IO	D30
0	IO	E18
0	IO_L0N	E28
0	IO_L0P	D29
0	IO_L1N_YY	D28
0	IO_L1P_YY	A31
0	IO_VREF_L2N_YY	E27
0	IO_L2P_YY	C29
0	IO_L3N_Y	B30
0	IO_L3P_Y	D27
0	IO_L4N_YY	E26
0	IO_L4P_YY	B29
0	IO_VREF_L5N_YY	D26
0	IO_L5P_YY	C27
0	IO_L6N	E25
0	IO_L6P	A28
0	IO_L7N_YY	D25
0	IO_L7P_YY	C26
0	IO_VREF_L8N_YY	E24[1]
0	IO_L8P_YY	B26
0	IO_L9N_Y	C25
0	IO_L9P_Y	D24
0	IO_VREF_L10N_YY	E23
0	IO_L10P_YY	A25
0	IO_L11N_YY	D23
0	IO_L11P_YY	B24
0	IO_L12N	E22
0	IO_L12P	C23
0	IO_L13N_YY	A23
0	IO_L13P_YY	D22
0	IO_VREF_L14N_YY	E21[1]
0	IO_L14P_YY	B22
0	IO_L15N_Y	D21
0	IO_L15P_Y	C21
0	IO_L16N_YY	B21
0	IO_L16P_YY	E20
0	IO_VREF_L17N_YY	D20
0	IO_L17P_YY	C20
0	IO_L18N	B20
0	IO_L18P	E19
0	IO_L19N_YY	D19
0	IO_L19P_YY	C19
0	IO_VREF_L20N_YY	A19
0	IO_L20P_YY	D18
0	IO_LVDS_DLL_L21N	C18
1	GCK2	D17
1	IO	A3
1	IO	D9
1	IO	E8
1	IO	E11
1	IO_LVDS_DLL_L21P	E17
1	IO_L22N_Y	C17
1	IO_L22P_Y	B17
1	IO_L23N_YY	B16
1	IO_VREF_L23P_YY	D16
1	IO_L24N_YY	E16
1	IO_L24P_YY	C16
1	IO_L25N	A15
1	IO_L25P	C15
1	IO_L26N_YY	D15
1	IO_VREF_L26P_YY	E15

Table 1: **BG560 BGA — XCV405E and XCV812E**

Bank	Pin Description	Pin#
1	IO_L27N_YY	C14
1	IO_L27P_YY	D14
1	IO_L28N_Y	A13
1	IO_L28P_Y	E14
1	IO_L29N_YY	C13
1	IO_VREF_L29P_YY	D13[1]
1	IO_L30N_YY	C12
1	IO_L30P_YY	E13
1	IO_L31N	A11
1	IO_L31P	D12
1	IO_L32N_YY	B11
1	IO_L32P_YY	C11
1	IO_L33N_YY	B10
1	IO_VREF_L33P_YY	D11
1	IO_L34N	C10
1	IO_L34P	A9
1	IO_L35N_YY	C9
1	IO_VREF_L35P_YY	D10[1]
1	IO_L36N_YY	A8
1	IO_L36P_YY	B8
1	IO_L37N_Y	E10
1	IO_L37P_Y	C8
1	IO_L38N_YY	B7
1	IO_VREF_L38P_YY	A6
1	IO_L39N_YY	C7
1	IO_L39P_YY	D8
1	IO_L40N	A5
1	IO_L40P	B5
1	IO_L41N_YY	C6
1	IO_VREF_L41P_YY	D7
1	IO_L42N_YY	A4
1	IO_L42P_YY	B4
1	IO_L43N_Y	C5
1	IO_L43P_Y	E7
1	IO_WRITE_L44N_YY	D6
1	IO_CS_L44P_YY	A2

Table 1: **BG560 BGA — XCV405E and XCV812E**

Bank	Pin Description	Pin#
2	IO	D3
2	IO	F3
2	IO	G1
2	IO	J2
2	IO_DOUT_BUSY_L45P_YY	D4
2	IO_DIN_D0_L45N_YY	E4
2	IO_L46P_Y	F5
2	IO_L46N_Y	B3
2	IO_L47P	F4
2	IO_L47N	C1
2	IO_VREF_L48P_Y	G5
2	IO_L48N_Y	E3
2	IO_L49P_Y	D2
2	IO_L49N_Y	G4
2	IO_L50P_Y	H5
2	IO_L50N_Y	E2
2	IO_VREF_L51P_YY	H4
2	IO_L51N_YY	G3
2	IO_L52P_Y	J5
2	IO_L52N_Y	F1
2	IO_L53P	J4
2	IO_L53N	H3
2	IO_VREF_L54P_YY	K5[1]
2	IO_L54N_YY	H2
2	IO_L55P_Y	J3
2	IO_L55N_Y	K4
2	IO_VREF_L56P_YY	L5
2	IO_D1_L56N_YY	K3
2	IO_D2_L57P_YY	L4
2	IO_L57N_YY	K2
2	IO_L58P_Y	M5
2	IO_L58N_Y	L3
2	IO_L59P	L1
2	IO_L59N	M4
2	IO_VREF_L60P_Y	N5[1]
2	IO_L60N_Y	M2
2	IO_L61P_Y	N4

Table 1: **BG560 BGA — XCV405E and XCV812E**

Bank	Pin Description	Pin#
2	IO_L61N_Y	N3
2	IO_L62P_Y	N2
2	IO_L62N_Y	P5
2	IO_VREF_L63P_YY	P4
2	IO_D3_L63N_YY	P3
2	IO_L64P_Y	P2
2	IO_L64N_Y	R5
2	IO_L65P_Y	R4
2	IO_L65N_Y	R3
2	IO_VREF_L66P_Y	R1
2	IO_L66N_Y	T4
2	IO_L67P_Y	T5
2	IO_L67N_Y	T3
2	IO_L68P_YY	T2
2	IO_L68N_YY	U3
3	IO	U4
3	IO	AE3
3	IO	AF3
3	IO	AH3
3	IO	AK3
3	IO_L69P_Y	U1
3	IO_L69N_Y	U2
3	IO_L70P_Y	V2
3	IO_VREF_L70N_Y	V4
3	IO_L71P_Y	V5
3	IO_L71N_Y	V3
3	IO_L72P	W1
3	IO_L72N	W3
3	IO_D4_L73P_YY	W4
3	IO_VREF_L73N_YY	W5
3	IO_L74P_Y	Y3
3	IO_L74N_Y	Y4
3	IO_L75P	AA1
3	IO_L75N	Y5
3	IO_L76P_Y	AA3
3	IO_VREF_L76N_Y	AA4[1]

Table 1: **BG560 BGA — XCV405E and XCV812E**

Bank	Pin Description	Pin#
3	IO_L77P	AB3
3	IO_L77N	AA5
3	IO_L78P	AC1
3	IO_L78N	AB4
3	IO_L79P_YY	AC3
3	IO_D5_L79N_YY	AB5
3	IO_D6_L80P_YY	AC4
3	IO_VREF_L80N_YY	AD3
3	IO_L81P_Y	AE1
3	IO_L81N_Y	AC5
3	IO_L82P_YY	AD4
3	IO_VREF_L82N_YY	AF1[1]
3	IO_L83P_Y	AF2
3	IO_L83N_Y	AD5
3	IO_L84P_Y	AG2
3	IO_L84N_Y	AE4
3	IO_L85P_YY	AH1
3	IO_VREF_L85N_YY	AE5
3	IO_L86P_Y	AF4
3	IO_L86N_Y	AJ1
3	IO_L87P_Y	AJ2
3	IO_L87N_Y	AF5
3	IO_L88P_Y	AG4
3	IO_VREF_L88N_Y	AK2
3	IO_L89P_Y	AJ3
3	IO_L89N_Y	AG5
3	IO_L90P_Y	AL1
3	IO_L90N_Y	AH4
3	IO_D7_L91P_YY	AJ4
3	IO_INIT_L91N_YY	AH5
4	GCK0	AL17
4	IO	AJ8
4	IO	AJ11
4	IO	AK6
4	IO	AK9
4	IO_L92P_YY	AL4

Table 1: **BG560 BGA — XCV405E and XCV812E**

Bank	Pin Description	Pin#
4	IO_L92N_YY	AJ6
4	IO_L93P	AK5
4	IO_L93N	AN3
4	IO_L94P_YY	AL5
4	IO_L94N_YY	AJ7
4	IO_VREF_L95P_YY	AM4
4	IO_L95N_YY	AM5
4	IO_L96P_Y	AK7
4	IO_L96N_Y	AL6
4	IO_L97P_YY	AM6
4	IO_L97N_YY	AN6
4	IO_VREF_L98P_YY	AL7
4	IO_L98N_YY	AJ9
4	IO_L99P	AN7
4	IO_L99N	AL8
4	IO_L100P_YY	AM8
4	IO_L100N_YY	AJ10
4	IO_VREF_L101P_YY	AL9[1]
4	IO_L101N_YY	AM9
4	IO_L102P_Y	AK10
4	IO_L102N_Y	AN9
4	IO_VREF_L103P_YY	AL10
4	IO_L103N_YY	AM10
4	IO_L104P_YY	AL11
4	IO_L104N_YY	AJ12
4	IO_L105P	AN11
4	IO_L105N	AK12
4	IO_L106P_YY	AL12
4	IO_L106N_YY	AM12
4	IO_VREF_L107P_YY	AK13[1]
4	IO_L107N_YY	AL13
4	IO_L108P_Y	AM13
4	IO_L108N_Y	AN13
4	IO_L109P_YY	AJ14
4	IO_L109N_YY	AK14
4	IO_VREF_L110P_YY	AM14
4	IO_L110N_YY	AN15
4	IO_L111P	AJ15
4	IO_L111N	AK15
4	IO_L112P_YY	AL15
4	IO_L112N_YY	AM16
4	IO_VREF_L113P_YY	AL16
4	IO_L113N_YY	AJ16
4	IO_L114P_Y	AK16
4	IO_L114N_Y	AN17
4	IO_LVDS_DLL_L115P	AM17
5	GCK1	AJ17
5	IO	AL18
5	IO	AL25
5	IO	AL28
5	IO	AL30
5	IO	AN28
5	IO_LVDS_DLL_L115N	AM18
5	IO_L116P_YY	AK18
5	IO_VREF_L116N_YY	AJ18
5	IO_L117P_YY	AN19
5	IO_L117N_YY	AL19
5	IO_L118P	AK19
5	IO_L118N	AM20
5	IO_L119P_YY	AJ19
5	IO_VREF_L119N_YY	AL20
5	IO_L120P_YY	AN21
5	IO_L120N_YY	AL21
5	IO_L121P_Y	AJ20
5	IO_L121N_Y	AM22
5	IO_L122P_YY	AK21
5	IO_VREF_L122N_YY	AN23[1]
5	IO_L123P_YY	AJ21
5	IO_L123N_YY	AM23
5	IO_L124P	AK22
5	IO_L124N	AM24
5	IO_L125P_YY	AL23
5	IO_L125N_YY	AJ22

Table 1: **BG560 BGA — XCV405E and XCV812E**

Bank	Pin Description	Pin#
5	IO_L126P_YY	AK23
5	IO_VREF_L126N_YY	AL24
5	IO_L127P_Y	AN26
5	IO_L127N_Y	AJ23
5	IO_L128P_YY	AK24
5	IO_VREF_L128N_YY	AM26[1]
5	IO_L129P_YY	AM27
5	IO_L129N_YY	AJ24
5	IO_L130P_Y	AL26
5	IO_L130N_Y	AK25
5	IO_L131P_YY	AN29
5	IO_VREF_L131N_YY	AJ25
5	IO_L132P_YY	AK26
5	IO_L132N_YY	AM29
5	IO_L133P_Y	AM30
5	IO_L133N_Y	AJ26
5	IO_L134P_YY	AK27
5	IO_VREF_L134N_YY	AL29
5	IO_L135P_YY	AN31
5	IO_L135N_YY	AJ27
5	IO_L136P_Y	AM31
5	IO_L136N_Y	AK28
6	IO	U29
6	IO	AE33
6	IO	AF31
6	IO	AJ32
6	IO	AL33
6	IO_L137N_YY	AH29
6	IO_L137P_YY	AJ30
6	IO_L138N_Y	AK31
6	IO_L138P_Y	AH30
6	IO_L139N_Y	AG29
6	IO_L139P_Y	AJ31
6	IO_VREF_L140N_Y	AK32
6	IO_L140P_Y	AG30
6	IO_L141N_Y	AH31

Table 1: **BG560 BGA — XCV405E and XCV812E**

Bank	Pin Description	Pin#
6	IO_L141P_Y	AF29
6	IO_L142N_Y	AH32
6	IO_L142P_Y	AF30
6	IO_VREF_L143N_YY	AE29
6	IO_L143P_YY	AH33
6	IO_L144N_Y	AG33
6	IO_L144P_Y	AE30
6	IO_L145N_Y	AD29
6	IO_L145P_Y	AF32
6	IO_VREF_L146N_Y	AE31[1]
6	IO_L146P_Y	AD30
6	IO_L147N_Y	AE32
6	IO_L147P_Y	AC29
6	IO_VREF_L148N_YY	AD31
6	IO_L148P_YY	AC30
6	IO_L149N_YY	AB29
6	IO_L149P_YY	AC31
6	IO_L150N_Y	AC33
6	IO_L150P_Y	AB30
6	IO_L151N_Y	AB31
6	IO_L151P_Y	AA29
6	IO_VREF_L152N_Y	AA30[1]
6	IO_L152P_Y	AA31
6	IO_L153N_Y	AA32
6	IO_L153P_Y	Y29
6	IO_L154N_Y	AA33
6	IO_L154P_Y	Y30
6	IO_VREF_L155N_YY	Y32
6	IO_L155P_YY	W29
6	IO_L156N_Y	W30
6	IO_L156P_Y	W31
6	IO_L157N_Y	W33
6	IO_L157P_Y	V30
6	IO_VREF_L158N_Y	V29
6	IO_L158P_Y	V31
6	IO_L159N_Y	V32
6	IO_L159P_Y	U33

Table 1: **BG560 BGA — XCV405E and XCV812E**

Bank	Pin Description	Pin#
7	IO	E30
7	IO	F29
7	IO	F33
7	IO	G30
7	IO	K30
7	IO_L160N_YY	U31
7	IO_L160P_YY	U32
7	IO_L161N_Y	T32
7	IO_L161P_Y	T30
7	IO_L162N_Y	T29
7	IO_VREF_L162P_Y	T31
7	IO_L163N_Y	R33
7	IO_L163P_Y	R31
7	IO_L164N_Y	R30
7	IO_L164P_Y	R29
7	IO_L165N_YY	P32
7	IO_VREF_L165P_YY	P31
7	IO_L166N_Y	P30
7	IO_L166P_Y	P29
7	IO_L167N_Y	M32
7	IO_L167P_Y	N31
7	IO_L168N_Y	N30
7	IO_VREF_L168P_Y	L33[1]
7	IO_L169N_Y	M31
7	IO_L169P_Y	L32
7	IO_L170N_Y	M30
7	IO_L170P_Y	L31
7	IO_L171N_YY	M29
7	IO_L171P_YY	J33
7	IO_L172N_YY	L30
7	IO_VREF_L172P_YY	K31
7	IO_L173N_Y	L29
7	IO_L173P_Y	H33
7	IO_L174N_Y	J31
7	IO_VREF_L174P_Y	H32[1]
7	IO_L175N_Y	K29

Table 1: **BG560 BGA — XCV405E and XCV812E**

Bank	Pin Description	Pin#
7	IO_L175P_Y	H31
7	IO_L176N_Y	J30
7	IO_L176P_Y	G32
7	IO_L177N_YY	J29
7	IO_VREF_L177P_YY	G31
7	IO_L178N_Y	E33
7	IO_L178P_Y	E32
7	IO_L179N_Y	H29
7	IO_L179P_Y	F31
7	IO_L180N_Y	D32
7	IO_VREF_L180P_Y	E31
7	IO_L181N_Y	G29
7	IO_L181P_Y	C33
7	IO_L182N_Y	F30
7	IO_L182P_Y	D31
2	CCLK	C4
3	DONE	AJ5
NA	DXN	AK29
NA	DXP	AJ28
NA	M0	AJ29
NA	M1	AK30
NA	M2	AN32
NA	PROGRAM	AM1
NA	TCK	E29
NA	TDI	D5
2	TDO	E6
NA	TMS	B33
NA	NC	C31
NA	NC	AC2
NA	NC	AK4
NA	NC	AL3
NA	VCCINT	A21
NA	VCCINT	B12
NA	VCCINT	B14

Table 1: **BG560 BGA — XCV405E and XCV812E**

Bank	Pin Description	Pin#
NA	VCCINT	B18
NA	VCCINT	B28
NA	VCCINT	C22
NA	VCCINT	C24
NA	VCCINT	E9
NA	VCCINT	E12
NA	VCCINT	F2
NA	VCCINT	H30
NA	VCCINT	J1
NA	VCCINT	K32
NA	VCCINT	M3
NA	VCCINT	N1
NA	VCCINT	N29
NA	VCCINT	N33
NA	VCCINT	U5
NA	VCCINT	U30
NA	VCCINT	Y2
NA	VCCINT	Y31
NA	VCCINT	AB2
NA	VCCINT	AB32
NA	VCCINT	AD2
NA	VCCINT	AD32
NA	VCCINT	AG3
NA	VCCINT	AG31
NA	VCCINT	AJ13
NA	VCCINT	AK8
NA	VCCINT	AK11
NA	VCCINT	AK17
NA	VCCINT	AK20
NA	VCCINT	AL14
NA	VCCINT	AL22
NA	VCCINT	AL27
NA	VCCINT	AN25
0	VCCO	A22
0	VCCO	A26
0	VCCO	A30

Table 1: **BG560 BGA — XCV405E and XCV812E**

Bank	Pin Description	Pin#
0	VCCO	B19
0	VCCO	B32
1	VCCO	A10
1	VCCO	A16
1	VCCO	B13
1	VCCO	C3
1	VCCO	E5
2	VCCO	B2
2	VCCO	D1
2	VCCO	H1
2	VCCO	M1
2	VCCO	R2
3	VCCO	V1
3	VCCO	AA2
3	VCCO	AD1
3	VCCO	AK1
3	VCCO	AL2
4	VCCO	AN4
4	VCCO	AN8
4	VCCO	AN12
4	VCCO	AM2
4	VCCO	AM15
5	VCCO	AL31
5	VCCO	AM21
5	VCCO	AN18
5	VCCO	AN24
5	VCCO	AN30
6	VCCO	W32
6	VCCO	AB33
6	VCCO	AF33
6	VCCO	AK33
6	VCCO	AM32
7	VCCO	C32
7	VCCO	D33
7	VCCO	K33
7	VCCO	N32
7	VCCO	T33

Table 1: **BG560 BGA — XCV405E and XCV812E**

Bank	Pin Description	Pin#
NA	GND	A1
NA	GND	A7
NA	GND	A12
NA	GND	A14
NA	GND	A18
NA	GND	A20
NA	GND	A24
NA	GND	A29
NA	GND	A32
NA	GND	A33
NA	GND	B1
NA	GND	B6
NA	GND	B9
NA	GND	B15
NA	GND	B23
NA	GND	B27
NA	GND	B31
NA	GND	C2
NA	GND	E1
NA	GND	F32
NA	GND	G2
NA	GND	G33
NA	GND	J32
NA	GND	K1
NA	GND	L2
NA	GND	M33
NA	GND	P1
NA	GND	P33
NA	GND	R32
NA	GND	T1
NA	GND	V33
NA	GND	W2
NA	GND	Y1
NA	GND	Y33
NA	GND	AB1
NA	GND	AC32

Table 1: **BG560 BGA — XCV405E and XCV812E**

Bank	Pin Description	Pin#
NA	GND	AD33
NA	GND	AE2
NA	GND	AG1
NA	GND	AG32
NA	GND	AH2
NA	GND	AJ33
NA	GND	AL32
NA	GND	AM3
NA	GND	AM7
NA	GND	AM11
NA	GND	AM19
NA	GND	AM25
NA	GND	AM28
NA	GND	AM33
NA	GND	AN1
NA	GND	AN2
NA	GND	AN5
NA	GND	AN10
NA	GND	AN14
NA	GND	AN16
NA	GND	AN20
NA	GND	AN22
NA	GND	AN27
NA	GND	AN33

Notes:
1. V_{REF} or I/O option only in the XCV812E.

BG560 Differential Pin Pairs

Virtex-E Extended Memory devices have differential pin pairs that can also provide other functions when not used as a differential pair. A √ in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package.

Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair is in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs that can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock.

Table 2: **BG560 Package Differential Pin Pair Summary XCV405E and XCV812E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
Global Differential Clock					
3	0	A17	C18	NA	IO LVDS 21
2	1	D17	E17	NA	IO LVDS 21
1	5	AJ17	AM18	NA	IO LVDS 115
0	4	AL17	AM17	NA	IO LVDS 115
IO LVDS Total Outputs: 183, Asyncronous Outputs: 79					
0	0	D29	E28	NA	-
1	0	A31	D28	√	-
2	0	C29	E27	√	VREF_0
3	0	D27	B30	1	-
4	0	B29	E26	√	-
5	0	C27	D26	√	VREF_0
6	0	A28	E25	NA	-
7	0	C26	D25	1	-
8	0	B26	E24	1	VREF_0
9	0	D24	C25	1	-
10	0	A25	E23	√	VREF_0
11	0	B24	D23	√	-
12	0	C23	E22	NA	-
13	0	D22	A23	√	-
14	0	B22	E21	√	VREF_0
15	0	C21	D21	1	-
16	0	E20	B21	√	-
17	0	C20	D20	√	VREF_0
18	0	E19	B20	NA	-
19	0	C19	D19	1	-
20	0	D18	A19	1	VREF_0
21	1	E17	C18	NA	GCLK LVDS 3/2
22	1	B17	C17	1	-
23	1	D16	B16	1	VREF_1
24	1	C16	E16	1	-
25	1	C15	A15	NA	-
26	1	E15	D15	√	VREF_1
27	1	D14	C14	√	-
28	1	E14	A13	1	-
29	1	D13	C13	√	VREF_1
30	1	E13	C12	√	-
31	1	D12	A11	NA	-
32	1	C11	B11	√	-
33	1	D11	B10	√	VREF_1
34	1	A9	C10	2	-
35	1	D10	C9	1	VREF_1
36	1	B8	A8	1	-
37	1	C8	E10	NA	-
38	1	A6	B7	√	VREF_1
39	1	D8	C7	√	-
40	1	B5	A5	2	-
41	1	D7	C6	√	VREF_1
42	1	B4	A4	√	-
43	1	E7	C5	NA	-
44	1	A2	D6	√	CS
45	2	D4	E4	√	DIN_D0
46	2	F5	B3	2	-
47	2	F4	C1	NA	-
48	2	G5	E3	1	VREF_2
49	2	D2	G4	1	-

Table 2: **BG560 Package Differential Pin Pair Summary XCV405E and XCV812E**

50	2	H5	E2	NA	-
51	2	H4	G3	√	VREF_2
52	2	J5	F1	NA	-
53	2	J4	H3	2	-
54	2	K5	H2	NA	VREF_2
55	2	J3	K4	NA	-
56	2	L5	K3	√	D1
57	2	L4	K2	√	D2
58	2	M5	L3	2	-
59	2	L1	M4	NA	-
60	2	N5	M2	1	VREF_2
61	2	N4	N3	1	-
62	2	N2	P5	NA	-
63	2	P4	P3	√	D3
64	2	P2	R5	2	-
65	2	R4	R3	NA	-
66	2	R1	T4	NA	VREF_2
67	2	T5	T3	NA	-
68	2	T2	U3	√	IRDY
69	3	U1	U2	NA	-
70	3	V2	V4	NA	VREF_3
71	3	V5	V3	NA	-
72	3	W1	W3	2	-
73	3	W4	W5	√	VREF_3
74	3	Y3	Y4	NA	-
75	3	AA1	Y5	1	-
76	3	AA3	AA4	1	VREF_3
77	3	AB3	AA5	NA	-
78	3	AC1	AB4	2	-
79	3	AC3	AB5	√	D5
80	3	AC4	AD3	√	VREF_3
81	3	AE1	AC5	1	-
82	3	AD4	AF1	NA	VREF_3
83	3	AF2	AD5	NA	-

Table 2: **BG560 Package Differential Pin Pair Summary XCV405E and XCV812E**

84	3	AG2	AE4	NA	-
85	3	AH1	AE5	√	VREF_3
86	3	AF4	AJ1	NA	-
87	3	AJ2	AF5	2	-
88	3	AG4	AK2	1	VREF_3
89	3	AJ3	AG5	NA	-
90	3	AL1	AH4	NA	-
91	3	AJ4	AH5	√	INIT
92	4	AL4	AJ6	√	-
93	4	AK5	AN3	NA	-
94	4	AL5	AJ7	√	-
95	4	AM4	AM5	√	VREF_4
96	4	AK7	AL6	1	-
97	4	AM6	AN6	√	-
98	4	AL7	AJ9	√	VREF_4
99	4	AN7	AL8	NA	-
100	4	AM8	AJ10	1	-
101	4	AL9	AM9	1	VREF_4
102	4	AK10	AN9	1	-
103	4	AL10	AM10	√	VREF_4
104	4	AL11	AJ12	√	-
105	4	AN11	AK12	NA	-
106	4	AL12	AM12	√	-
107	4	AK13	AL13	√	VREF_4
108	4	AM13	AN13	1	-
109	4	AJ14	AK14	√	-
110	4	AM14	AN15	√	VREF_4
111	4	AJ15	AK15	NA	-
112	4	AL15	AM16	1	-
113	4	AL16	AJ16	1	VREF_4
114	4	AK16	AN17	1	-
115	5	AM17	AM18	NA	GCLK LVDS 1/0
116	5	AK18	AJ18	1	VREF_5
117	5	AN19	AL19	1	-

Table 2: **BG560 Package Differential Pin Pair Summary XCV405E and XCV812E**

118	5	AK19	AM20	NA	-
119	5	AJ19	AL20	√	VREF_5
120	5	AN21	AL21	√	-
121	5	AJ20	AM22	1	-
122	5	AK21	AN23	√	VREF_5
123	5	AJ21	AM23	√	-
124	5	AK22	AM24	NA	-
125	5	AL23	AJ22	√	-
126	5	AK23	AL24	√	VREF_5
127	5	AN26	AJ23	2	-
128	5	AK24	AM26	1	VREF_5
129	5	AM27	AJ24	1	-
130	5	AL26	AK25	NA	-
131	5	AN29	AJ25	√	VREF_5
132	5	AK26	AM29	√	-
133	5	AM30	AJ26	2	-
134	5	AK27	AL29	√	VREF_5
135	5	AN31	AJ27	√	-
136	5	AM31	AK28	NA	-
137	6	AJ30	AH29	√	-
138	6	AH30	AK31	2	-
139	6	AJ31	AG29	NA	-
140	6	AG30	AK32	1	VREF_6
141	6	AF29	AH31	1	-
142	6	AF30	AH32	NA	-
143	6	AH33	AE29	√	VREF_6
144	6	AE30	AG33	2	-
145	6	AF32	AD29	NA	-
146	6	AD30	AE31	NA	VREF_6
147	6	AC29	AE32	NA	-
148	6	AC30	AD31	√	VREF_6
149	6	AC31	AB29	√	-
150	6	AB30	AC33	2	-
151	6	AA29	AB31	NA	-

Table 2: **BG560 Package Differential Pin Pair Summary XCV405E and XCV812E**

152	6	AA31	AA30	1	VREF_6
153	6	Y29	AA32	1	-
154	6	Y30	AA33	NA	-
155	6	W29	Y32	√	VREF_6
156	6	W31	W30	2	-
157	6	V30	W33	NA	-
158	6	V31	V29	NA	VREF_6
159	6	U33	V32	NA	-
160	7	U32	U31	√	IRDY
161	7	T30	T32	NA	-
162	7	T31	T29	NA	VREF_7
163	7	R31	R33	NA	-
164	7	R29	R30	2	-
165	7	P31	P32	√	VREF_7
166	7	P29	P30	NA	-
167	7	N31	M32	1	-
168	7	L33	N30	1	VREF_7
169	7	L32	M31	NA	-
170	7	L31	M30	2	-
171	7	J33	M29	√	-
172	7	K31	L30	√	VREF_7
173	7	H33	L29	1	-
174	7	H32	J31	NA	VREF_7
175	7	H31	K29	NA	-
176	7	G32	J30	NA	-
177	7	G31	J29	√	VREF_7
178	7	E32	E33	NA	-
179	7	F31	H29	2	-
180	7	E31	D32	1	VREF_7
181	7	C33	G29	NA	-
182	7	D31	F30	NA	-

Notes:
1. AO in the XCV812E
2. AO in the XCV405E

FG676 Fine-Pitch Ball Grid Array Package

XCV405E Virtex-E Extended Memory devices are available in the FG676 fine-pitch BGA package. Pins labeled I0_VREF can be used as either. If the pin is not used as V_{REF}, it can be used as general I/O. Immediately following Table 3, see Table 4 for FG676 package Differential Pair information.

Table 3: **FG676 Fine-Pitch BGA — XCV405E**

Bank	Pin Description	Pin #
0	GCK3	E13
0	IO	A6
0	IO	B3
0	IO	C6
0	IO	C8
0	IO	D5
0	IO	G13
0	IO_L0N_Y	C4
0	IO_L0P_Y	F7
0	IO_L1N_YY	G8
0	IO_L1P_YY	C5
0	IO_VREF_L2N_YY	D6
0	IO_L2P_YY	E7
0	IO_L3N	A4
0	IO_L3P	F8
0	IO_L4N	B5
0	IO_L4P	D7
0	IO_VREF_L5N_YY	E8
0	IO_L5P_YY	G9
0	IO_L6N_YY	A5
0	IO_L6P_YY	F9
0	IO_L7N_Y	D8
0	IO_L7P_Y	C7
0	IO_L8N_Y	B7
0	IO_L8P_Y	E9
0	IO_L9N	A7
0	IO_L9P	D9
0	IO_L10N	B8
0	IO_VREF_L10P	G10
0	IO_L11N_YY	C9
0	IO_L11P_YY	F10
0	IO_L12N_Y	A8
0	IO_L12P_Y	E10
0	IO_L13N_YY	G11
0	IO_L13P_YY	D10
0	IO_L14N_YY	B10
0	IO_L14P_YY	F11
0	IO_L15N	C10
0	IO_L15P	E11
0	IO_L16N_YY	G12
0	IO_L16P_YY	D11
0	IO_VREF_L17N_YY	C11
0	IO_L17P_YY	F12
0	IO_L18N_YY	A11
0	IO_L18P_YY	E12
0	IO_L19N_Y	D12
0	IO_L19P_Y	C12
0	IO_VREF_L20N_Y	A12
0	IO_L20P_Y	H13
0	IO_LVDS_DLL_L21N	B13
1	GCK2	C13
1	IO	A19
1	IO	A20
1	IO	A22
1	IO	B23
1	IO_LVDS_DLL_L21P	F14
1	IO_L22N	E14
1	IO_L22P	F13
1	IO_L23N_Y	D14
1	IO_VREF_L23P_Y	A14
1	IO_L24N_Y	C14
1	IO_L24P_Y	H14
1	IO_L25N_YY	G14

Table 3: **FG676 Fine-Pitch BGA — XCV405E**

Bank	Pin Description	Pin #
1	IO_L25P_YY	C15
1	IO_L26N_YY	E15
1	IO_VREF_L26P_YY	D15
1	IO_L27N_YY	C16
1	IO_L27P_YY	F15
1	IO_L28N	G15
1	IO_L28P	D16
1	IO_L29N_YY	E16
1	IO_L29P_YY	A17
1	IO_L30N_YY	C17
1	IO_L30P_YY	E17
1	IO_L31N_Y	F16
1	IO_L31P_Y	D17
1	IO_L32N_YY	F17
1	IO_L32P_YY	C18
1	IO_L33N_YY	A18
1	IO_VREF_L33P_YY	G16
1	IO_L34N_YY	C19
1	IO_L34P_YY	G17
1	IO_L35N_Y	D18
1	IO_L35P_Y	B19
1	IO_L36N_Y	D19
1	IO_L36P_Y	E18
1	IO_L37N_YY	F18
1	IO_L37P_YY	B20
1	IO_L38N_YY	G19
1	IO_VREF_L38P_YY	C20
1	IO_L39N_YY	G18
1	IO_L39P_YY	E19
1	IO_L40N_YY	A21
1	IO_L40P_YY	D20
1	IO_L41N_YY	F19
1	IO_VREF_L41P_YY	C21
1	IO_L42N_YY	B22
1	IO_L42P_YY	E20

Table 3: **FG676 Fine-Pitch BGA — XCV405E**

Bank	Pin Description	Pin #
1	IO_L43N_Y	A23
1	IO_L43P_Y	D21
1	IO_WRITE_L44N_YY	C22
1	IO_CS_L44P_YY	E21
2	IO	D26
2	IO	E26
2	IO	F26
2	IO_D1	K24
2	IO_DOUT_BUSY_L45P_YY	E23
2	IO_DIN_D0_L45N_YY	F22
2	IO_L46P_YY	E24
2	IO_L46N_YY	F20
2	IO_L47P_Y	G21
2	IO_L47N_Y	G22
2	IO_VREF_L48P_Y	F24
2	IO_L48N_Y	H20
2	IO_L49P_Y	E25
2	IO_L49N_Y	H21
2	IO_L50P_YY	F23
2	IO_L50N_YY	G23
2	IO_VREF_L51P_YY	H23
2	IO_L51N_YY	J20
2	IO_L52P_YY	G24
2	IO_L52N_YY	H22
2	IO_L53P_Y	J21
2	IO_L53N_Y	G25
2	IO_L54P_Y	G26
2	IO_L54N_Y	J22
2	IO_L55P_YY	H24
2	IO_L55N_YY	J23
2	IO_L56P_YY	J24
2	IO_VREF_L56N_YY	K20
2	IO_D2_L57P_YY	K22
2	IO_L57N_YY	K21

Table 3: **FG676 Fine-Pitch BGA — XCV405E**

Bank	Pin Description	Pin #
2	IO_L58P_YY	H25
2	IO_L58N_YY	K23
2	IO_L59P_Y	L20
2	IO_L59N_Y	J26
2	IO_L60P_Y	K25
2	IO_L60N_Y	L22
2	IO_L61P_Y	L21
2	IO_L61N_Y	L23
2	IO_L62P_Y	M20
2	IO_L62N_Y	L24
2	IO_VREF_L63P_YY	M23
2	IO_D3_L63N_YY	M22
2	IO_L64P_YY	L26
2	IO_L64N_YY	M21
2	IO_L65P_Y	N19
2	IO_L65N_Y	M24
2	IO_VREF_L66P_Y	M26
2	IO_L66N_Y	N20
2	IO_L67P_YY	N24
2	IO_L67N_YY	N21
2	IO_L68P_YY	N23
2	IO_L68N_YY	N22
3	IO	P24
3	IO	W25
3	IO	Y26
3	IO	AB25
3	IO	AC26
3	IO_L69P_YY	P21
3	IO_L69N_YY	P23
3	IO_L70P_Y	P22
3	IO_VREF_L70N_Y	R25
3	IO_L71P_Y	P19
3	IO_L71N_Y	P20
3	IO_L72P_YY	R21

Table 3: **FG676 Fine-Pitch BGA — XCV405E**

Bank	Pin Description	Pin #
3	IO_L72N_YY	R22
3	IO_D4_L73P_YY	R24
3	IO_VREF_L73N_YY	R23
3	IO_L74P_Y	T24
3	IO_L74N_Y	R20
3	IO_L75P_Y	T22
3	IO_L75N_Y	U24
3	IO_L76P_Y	T23
3	IO_L76N_Y	U25
3	IO_L77P_Y	T21
3	IO_L77N_Y	U20
3	IO_L78P_YY	U22
3	IO_L78N_YY	V26
3	IO_L79P_YY	T20
3	IO_D5_L79N_YY	U23
3	IO_D6_L80P_YY	V24
3	IO_VREF_L80N_YY	U21
3	IO_L81P_YY	V23
3	IO_L81N_YY	W24
3	IO_L82P_Y	V22
3	IO_L82N_Y	W26
3	IO_L83P_Y	Y25
3	IO_L83N_Y	V21
3	IO_L84P_YY	V20
3	IO_L84N_YY	AA26
3	IO_L85P_YY	Y24
3	IO_VREF_L85N_YY	W23
3	IO_L86P_Y	AA24
3	IO_L86N_Y	Y23
3	IO_L87P_Y	AB26
3	IO_L87N_Y	W21
3	IO_L88P_Y	Y22
3	IO_VREF_L88N_Y	W22
3	IO_L89P_Y	AA23
3	IO_L89N_Y	AB24

Table 3: **FG676 Fine-Pitch BGA — XCV405E**

Bank	Pin Description	Pin #
3	IO_L90P_YY	W20
3	IO_L90N_YY	AC24
3	IO_D7_L91P_YY	AB23
3	IO_INIT_L91N_YY	Y21
4	GCK0	AA14
4	IO	AC18
4	IO	AE20
4	IO	AE23
4	IO	AF21
4	IO_L92P_YY	AC22
4	IO_L92N_YY	AD26
4	IO_L93P_Y	AD23
4	IO_L93N_Y	AA20
4	IO_L94P_YY	Y19
4	IO_L94N_YY	AC21
4	IO_VREF_L95P_YY	AD22
4	IO_L95N_YY	AB20
4	IO_L96P	AE22
4	IO_L96N	Y18
4	IO_L97P	AF22
4	IO_L97N	AA19
4	IO_VREF_L98P_YY	AD21
4	IO_L98N_YY	AB19
4	IO_L99P_YY	AC20
4	IO_L99N_YY	AA18
4	IO_L100P_Y	AC19
4	IO_L100N_Y	AD20
4	IO_L101P_Y	AF20
4	IO_L101N_Y	AB18
4	IO_L102P	AD19
4	IO_L102N	Y17
4	IO_L103P	AE19
4	IO_VREF_L103N	AD18
4	IO_L104P_YY	AF19

Table 3: **FG676 Fine-Pitch BGA — XCV405E**

Bank	Pin Description	Pin #
4	IO_L104N_YY	AA17
4	IO_L105P_Y	AC17
4	IO_L105N_Y	AB17
4	IO_L106P_YY	Y16
4	IO_L106N_YY	AE17
4	IO_L107P_YY	AF17
4	IO_L107N_YY	AA16
4	IO_L108P	AD17
4	IO_L108N	AB16
4	IO_L109P_YY	AC16
4	IO_L109N_YY	AD16
4	IO_VREF_L110P_YY	AC15
4	IO_L110N_YY	Y15
4	IO_L111P_YY	AD15
4	IO_L111N_YY	AA15
4	IO_L112P_Y	W14
4	IO_L112N_Y	AB15
4	IO_VREF_L113P_Y	AF15
4	IO_L113N_Y	Y14
4	IO_L114P	AD14
4	IO_L114N	AB14
4	IO_LVDS_DLL_L115P	AC14
5	GCK1	AB13
5	IO	AD7
5	IO	AD13
5	IO	AE4
5	IO	AE7
5	IO	AF5
5	IO_LVDS_DLL_L115N	AF13
5	IO_L116P_Y	AA13
5	IO_VREF_L116N_Y	AF12
5	IO_L117P_Y	AC13
5	IO_L117N_Y	W13
5	IO_L118P_YY	AA12

Table 3: **FG676 Fine-Pitch BGA — XCV405E**

Bank	Pin Description	Pin #
5	IO_L118N_YY	AD12
5	IO_L119P_YY	AC12
5	IO_VREF_L119N_YY	AB12
5	IO_L120P_YY	AD11
5	IO_L120N_YY	Y12
5	IO_L121P	AB11
5	IO_L121N	AD10
5	IO_L122P_YY	AC11
5	IO_L122N_YY	AE10
5	IO_L123P_YY	AC10
5	IO_L123N_YY	AA11
5	IO_L124P_Y	Y11
5	IO_L124N_Y	AD9
5	IO_L125P_YY	AB10
5	IO_L125N_YY	AF9
5	IO_L126P_YY	AD8
5	IO_VREF_L126N_YY	AA10
5	IO_L127P_YY	AE8
5	IO_L127N_YY	Y10
5	IO_L128P_Y	AC9
5	IO_L128N_Y	AF8
5	IO_L129P_Y	AF7
5	IO_L129N_Y	AB9
5	IO_L130P_YY	AA9
5	IO_L130N_YY	AF6
5	IO_L131P_YY	AC8
5	IO_VREF_L131N_YY	AC7
5	IO_L132P_YY	AD6
5	IO_L132N_YY	Y9
5	IO_L133P_YY	AE5
5	IO_L133N_YY	AA8
5	IO_L134P_YY	AC6
5	IO_VREF_L134N_YY	AB8
5	IO_L135P_YY	AD5
5	IO_L135N_YY	AA7

Table 3: **FG676 Fine-Pitch BGA — XCV405E**

Bank	Pin Description	Pin #
5	IO_L136P_Y	AF4
5	IO_L136N_Y	AC5
6	IO	P3
6	IO	AA3
6	IO	W3
6	IO	Y2
6	IO	Y6
6	IO_L137N_YY	AA5
6	IO_L137P_YY	AC3
6	IO_L138N_YY	AC2
6	IO_L138P_YY	AB4
6	IO_L139N_Y	W6
6	IO_L139P_Y	AA4
6	IO_VREF_L140N_Y	AB3
6	IO_L140P_Y	Y5
6	IO_L141N_Y	AB2
6	IO_L141P_Y	V7
6	IO_L142N_YY	AB1
6	IO_L142P_YY	Y4
6	IO_VREF_L143N_YY	V5
6	IO_L143P_YY	W5
6	IO_L144N_YY	AA1
6	IO_L144P_YY	V6
6	IO_L145N_Y	W4
6	IO_L145P_Y	Y3
6	IO_L146N_Y	Y1
6	IO_L146P_Y	U7
6	IO_L147N_YY	W1
6	IO_L147P_YY	V4
6	IO_L148N_YY	W2
6	IO_VREF_L148P_YY	U6
6	IO_L149N_YY	V3
6	IO_L149P_YY	T5
6	IO_L150N_YY	U5

Table 3: **FG676 Fine-Pitch BGA — XCV405E**

Bank	Pin Description	Pin #
6	IO_L150P_YY	U4
6	IO_L151N_Y	T7
6	IO_L151P_Y	U3
6	IO_L152N_Y	U2
6	IO_L152P_Y	T6
6	IO_L153N_Y	U1
6	IO_L153P_Y	T4
6	IO_L154N_Y	R7
6	IO_L154P_Y	T3
6	IO_VREF_L155N_YY	R4
6	IO_L155P_YY	R6
6	IO_L156N_YY	R3
6	IO_L156P_YY	R5
6	IO_L157N_Y	P8
6	IO_L157P_Y	P7
6	IO_VREF_L158N_Y	R1
6	IO_L158P_Y	P6
6	IO_L159N_YY	P5
6	IO_L159P_YY	P4
7	IO	D2
7	IO	D3
7	IO	E1
7	IO	G1
7	IO	H2
7	IO_L160N_YY	N5
7	IO_L160P_YY	N8
7	IO_L161N_YY	N6
7	IO_L161P_YY	N3
7	IO_L162N_Y	N4
7	IO_VREF_L162P_Y	M2
7	IO_L163N_Y	N7
7	IO_L163P_Y	M7
7	IO_L164N_YY	M6
7	IO_L164P_YY	M3

Table 3: **FG676 Fine-Pitch BGA — XCV405E**

Bank	Pin Description	Pin #
7	IO_L165N_YY	M4
7	IO_VREF_L165P_YY	M5
7	IO_L166N_Y	L3
7	IO_L166P_Y	L7
7	IO_L167N_Y	L6
7	IO_L167P_Y	K2
7	IO_L168N_Y	L4
7	IO_L168P_Y	K1
7	IO_L169N_Y	K3
7	IO_L169P_Y	L5
7	IO_L170N_YY	K5
7	IO_L170P_YY	J3
7	IO_L171N_YY	K4
7	IO_L171P_YY	J4
7	IO_L172N_YY	H3
7	IO_VREF_L172P_YY	K6
7	IO_L173N_YY	K7
7	IO_L173P_YY	G3
7	IO_L174N_Y	J5
7	IO_L174P_Y	H1
7	IO_L175N_Y	G2
7	IO_L175P_Y	J6
7	IO_L176N_YY	J7
7	IO_L176P_YY	F1
7	IO_L177N_YY	H4
7	IO_VREF_L177P_YY	G4
7	IO_L178N_Y	F3
7	IO_L178P_Y	H5
7	IO_L179N_Y	E2
7	IO_L179P_Y	H6
7	IO_L180N_Y	G5
7	IO_VREF_L180P_Y	F4
7	IO_L181N_Y	H7
7	IO_L181P_Y	G6
7	IO_L182N_YY	E3

Table 3: **FG676 Fine-Pitch BGA — XCV405E**

Bank	Pin Description	Pin #
7	IO_L182P_YY	E4
2	CCLK	D24
3	DONE	AB21
NA	DXN	AB7
NA	DXP	Y8
NA	M0	AD4
NA	M1	W7
NA	M2	AB6
NA	PROGRAM	AA22
NA	TCK	E6
NA	TDI	D22
2	TDO	C23
NA	TMS	F5
0	NC	A9
0	NC	A10
0	NC	B4
0	NC	B12
0	NC	D13
1	NC	A13
1	NC	A16
1	NC	A24
1	NC	B15
1	NC	B17
2	NC	D25
2	NC	H26
2	NC	K26
2	NC	M25
2	NC	N26
3	NC	AC25
3	NC	P26
3	NC	R26
3	NC	T26
3	NC	U26

Table 3: **FG676 Fine-Pitch BGA — XCV405E**

Bank	Pin Description	Pin #
4	NC	AE15
4	NC	AF14
4	NC	AF16
4	NC	AF18
4	NC	AF23
5	NC	AE12
5	NC	AF3
5	NC	AF10
5	NC	AF11
5	NC	Y13
6	NC	AC1
6	NC	P1
6	NC	R2
6	NC	T1
6	NC	V1
7	NC	D1
7	NC	J1
7	NC	L1
7	NC	M1
7	NC	N1
NA	NC	T25
NA	NC	T2
NA	NC	P2
NA	NC	N25
NA	NC	L25
NA	NC	L2
NA	NC	F6
NA	NC	F25
NA	NC	F21
NA	NC	F2
NA	NC	C26
NA	NC	C25
NA	NC	C2
NA	NC	C1
NA	NC	B6

Table 3: **FG676 Fine-Pitch BGA — XCV405E**

Bank	Pin Description	Pin #
NA	NC	B26
NA	NC	B24
NA	NC	B21
NA	NC	B16
NA	NC	B11
NA	NC	B1
NA	NC	AF25
NA	NC	AF24
NA	NC	AF2
NA	NC	AE6
NA	NC	AE3
NA	NC	AE26
NA	NC	AE24
NA	NC	AE21
NA	NC	AE16
NA	NC	AE14
NA	NC	AE11
NA	NC	AE1
NA	NC	AD25
NA	NC	AD2
NA	NC	AD1
NA	NC	AA6
NA	NC	AA25
NA	NC	AA21
NA	NC	AA2
NA	NC	A3
NA	NC	A25
NA	NC	A2
NA	NC	A15
NA	VCCINT	G7
NA	VCCINT	G20
NA	VCCINT	H8
NA	VCCINT	H19
NA	VCCINT	J9

Table 3: **FG676 Fine-Pitch BGA — XCV405E**

Bank	Pin Description	Pin #
NA	VCCINT	J10
NA	VCCINT	J11
NA	VCCINT	J16
NA	VCCINT	J17
NA	VCCINT	J18
NA	VCCINT	K9
NA	VCCINT	K18
NA	VCCINT	L9
NA	VCCINT	L18
NA	VCCINT	T9
NA	VCCINT	T18
NA	VCCINT	U9
NA	VCCINT	U18
NA	VCCINT	V9
NA	VCCINT	V10
NA	VCCINT	V11
NA	VCCINT	V16
NA	VCCINT	V17
NA	VCCINT	V18
NA	VCCINT	Y7
NA	VCCINT	Y20
NA	VCCINT	W8
NA	VCCINT	W19
0	VCCO	J13
0	VCCO	J12
0	VCCO	H9
0	VCCO	H12
0	VCCO	H11
0	VCCO	H10
1	VCCO	J15
1	VCCO	J14
1	VCCO	H18
1	VCCO	H17
1	VCCO	H16

Table 3: **FG676 Fine-Pitch BGA — XCV405E**

Bank	Pin Description	Pin #
1	VCCO	H15
2	VCCO	N18
2	VCCO	M19
2	VCCO	M18
2	VCCO	L19
2	VCCO	K19
2	VCCO	J19
3	VCCO	V19
3	VCCO	U19
3	VCCO	T19
3	VCCO	R19
3	VCCO	R18
3	VCCO	P18
4	VCCO	W18
4	VCCO	W17
4	VCCO	W16
4	VCCO	W15
4	VCCO	V15
4	VCCO	V14
5	VCCO	W9
5	VCCO	W12
5	VCCO	W11
5	VCCO	W10
5	VCCO	V13
5	VCCO	V12
6	VCCO	V8
6	VCCO	U8
6	VCCO	T8
6	VCCO	R9
6	VCCO	R8
6	VCCO	P9
7	VCCO	N9
7	VCCO	M9
7	VCCO	M8
7	VCCO	L8

Table 3: **FG676 Fine-Pitch BGA — XCV405E**

Bank	Pin Description	Pin #
7	VCCO	K8
7	VCCO	J8
NA	GND	V25
NA	GND	V2
NA	GND	U17
NA	GND	U16
NA	GND	U15
NA	GND	U14
NA	GND	U13
NA	GND	U12
NA	GND	U11
NA	GND	U10
NA	GND	T17
NA	GND	T16
NA	GND	T15
NA	GND	T14
NA	GND	T13
NA	GND	T12
NA	GND	T11
NA	GND	T10
NA	GND	R17
NA	GND	R16
NA	GND	R15
NA	GND	R14
NA	GND	R13
NA	GND	R12
NA	GND	R11
NA	GND	R10
NA	GND	P25
NA	GND	P17
NA	GND	P16
NA	GND	P15
NA	GND	P14
NA	GND	P13

Table 3: **FG676 Fine-Pitch BGA — XCV405E**

Bank	Pin Description	Pin #
NA	GND	P12
NA	GND	P11
NA	GND	P10
NA	GND	N2
NA	GND	N17
NA	GND	N16
NA	GND	N15
NA	GND	N14
NA	GND	N13
NA	GND	N12
NA	GND	N11
NA	GND	N10
NA	GND	M17
NA	GND	M16
NA	GND	M15
NA	GND	M14
NA	GND	M13
NA	GND	M12
NA	GND	M11
NA	GND	M10
NA	GND	L17
NA	GND	L16
NA	GND	L15
NA	GND	L14
NA	GND	L13
NA	GND	L12
NA	GND	L11
NA	GND	L10
NA	GND	K17
NA	GND	K16
NA	GND	K15
NA	GND	K14
NA	GND	K13
NA	GND	K12
NA	GND	K11

Table 3: **FG676 Fine-Pitch BGA — XCV405E**

Bank	Pin Description	Pin #
NA	GND	K10
NA	GND	J25
NA	GND	J2
NA	GND	E5
NA	GND	E22
NA	GND	D4
NA	GND	D23
NA	GND	C3
NA	GND	C24
NA	GND	B9
NA	GND	B25
NA	GND	B2
NA	GND	B18
NA	GND	B14
NA	GND	AF26
NA	GND	AF1
NA	GND	AE9
NA	GND	AE25
NA	GND	AE2
NA	GND	AE18
NA	GND	AE13
NA	GND	AD3
NA	GND	AD24
NA	GND	AC4
NA	GND	AC23
NA	GND	AB5
NA	GND	AB22
NA	GND	A26
NA	GND	A1

FG676 Differential Pin Pairs

Virtex-E Extended Memory devices have differential pin pairs that can also provide other functions when not used as a differential pair. A √ in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package.

Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair is in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs that can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock.

Table 4: **FG676 Fine-Pitch BGA Differential Pin Pair Summary — XCV405E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
Global Differential Clock					
3	0	E13	B13	NA	IO_DLL_L21N
2	1	C13	F14	NA	IO_DLL_L21P
1	5	AB13	AF13	NA	IO_DLL_L115N
0	4	AA14	AC14	NA	IO_DLL_L115P
IOLVDS Total Pairs: 183, Asynchronous Output Pairs: 97					
0	0	F7	C4	NA	-
1	0	C5	G8	√	-
2	0	E7	D6	√	VREF
3	0	F8	A4	NA	-
4	0	D7	B5	NA	-
5	0	G9	E8	√	VREF
6	0	F9	A5	√	-
7	0	C7	D8	NA	-
8	0	E9	B7	NA	-
9	0	D9	A7	NA	-
10	0	G10	B8	NA	VREF
11	0	F10	C9	√	-
12	0	E10	A8	NA	-
13	0	D10	G11	√	-
14	0	F11	B10	√	-
15	0	E11	C10	NA	-

Table 4: **FG676 Fine-Pitch BGA Differential Pin Pair Summary — XCV405E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
16	0	D11	G12	√	-
17	0	F12	C11	√	VREF
18	0	E12	A11	√	-
19	0	C12	D12	NA	-
20	0	H13	A12	NA	VREF
21	1	F14	B13	NA	IO_LVDS_DLL
22	1	F13	E14	NA	-
23	1	A14	D14	NA	VREF
24	1	H14	C14	NA	-
25	1	C15	G14	√	-
26	1	D15	E15	√	VREF
27	1	F15	C16	√	-
28	1	D16	G15	-	-
29	1	A17	E16	√	-
30	1	E17	C17	√	-
31	1	D17	F16	NA	-
32	1	C18	F17	√	-
33	1	G16	A18	√	VREF
34	1	G17	C19	√	-
35	1	B19	D18	NA	-
36	1	E18	D19	NA	-
37	1	B20	F18	√	-
38	1	C20	G19	√	VREF
39	1	E19	G18	√	-
40	1	D20	A21	√	-
41	1	C21	F19	√	VREF
42	1	E20	B22	√	-
43	1	D21	A23	2	-
44	1	E21	C22	√	CS
45	2	E23	F22	√	DIN, D0
46	2	E24	F20	√	-
47	2	G21	G22	2	-
48	2	F24	H20	1	VREF
49	2	E25	H21	1	-

Table 4: **FG676 Fine-Pitch BGA Differential Pin Pair Summary — XCV405E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
50	2	F23	G23	√	-
51	2	H23	J20	√	VREF
52	2	G24	H22	√	-
53	2	J21	G25	2	-
54	2	G26	J22	1	-
55	2	H24	J23	√	-
56	2	J24	K20	√	VREF
57	2	K22	K21	√	D2
58	2	H25	K23	√	-
59	2	L20	J26	2	-
60	2	K25	L22	1	-
61	2	L21	L23	1	-
62	2	M20	L24	1	-
63	2	M23	M22	√	D3
64	2	L26	M21	√	-
65	2	N19	M24	2	-
66	2	M26	N20	1	VREF
67	2	N24	N21	√	-
68	2	N23	N22	√	-
69	3	P21	P23	√	-
70	3	P22	R25	1	VREF
71	3	P19	P20	2	-
72	3	R21	R22	√	-
73	3	R24	R23	√	VREF
74	3	T24	R20	1	-
75	3	T22	U24	1	-
76	3	T23	U25	1	-
77	3	T21	U20	2	-
78	3	U22	V26	√	-
79	3	T20	U23	√	D5
80	3	V24	U21	√	VREF
81	3	V23	W24	√	-
82	3	V22	W26	NA	-
83	3	Y25	V21	NA	-

Table 4: **FG676 Fine-Pitch BGA Differential Pin Pair Summary — XCV405E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
84	3	V20	AA26	√	-
85	3	Y24	W23	√	VREF
86	3	AA24	Y23	NA	-
87	3	AB26	W21	NA	-
88	3	Y22	W22	NA	VREF
89	3	AA23	AB24	NA	-
90	3	W20	AC24	√	-
91	3	AB23	Y21	√	INIT
92	4	AC22	AD26	√	-
93	4	AD23	AA20	NA1	-
94	4	Y19	AC21	√	-
95	4	AD22	AB20	√	VREF
96	4	AE22	Y18	NA	-
97	4	AF22	AA19	NA	-
98	4	AD21	AB19	√	VREF
99	4	AC20	AA18	√	-
100	4	AC19	AD20	NA	-
101	4	AF20	AB18	NA	-
102	4	AD19	Y17	NA	-
103	4	AE19	AD18	NA	VREF
104	4	AF19	AA17	√	-
105	4	AC17	AB17	NA	-
106	4	Y16	AE17	√	-
107	4	AF17	AA16	√	-
108	4	AD17	AB16	NA	-
109	4	AC16	AD16	√	-
110	4	AC15	Y15	√	VREF
111	4	AD15	AA15	√	-
112	4	W14	AB15	NA	-
113	4	AF15	Y14	NA	VREF
114	4	AD14	AB14	NA	-
115	5	AC14	AF13	NA	IO_LVDS_DLL
116	5	AA13	AF12	NA	VREF
117	5	AC13	W13	NA	-

Table 4: **FG676 Fine-Pitch BGA Differential Pin Pair Summary — XCV405E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
118	5	AA12	AD12	√	-
119	5	AC12	AB12	√	VREF
120	5	AD11	Y12	√	-
121	5	AB11	AD10	NA	-
122	5	AC11	AE10	√	-
123	5	AC10	AA11	√	-
124	5	Y11	AD9	NA	-
125	5	AB10	AF9	√	-
126	5	AD8	AA10	√	VREF
127	5	AE8	Y10	√	-
128	5	AC9	AF8	NA	-
129	5	AF7	AB9	NA	-
130	5	AA9	AF6	√	-
131	5	AC8	AC7	√	VREF
132	5	AD6	Y9	√	-
133	5	AE5	AA8	√	-
134	5	AC6	AB8	√	VREF
135	5	AD5	AA7	√	-
136	5	AF4	AC5	NA	-
137	6	AC3	AA5	√	-
138	6	AB4	AC2	√	-
139	6	AA4	W6	NA	-
140	6	Y5	AB3	NA	VREF
141	6	V7	AB2	NA	-
142	6	Y4	AB1	√	-
143	6	W5	V5	√	VREF
144	6	V6	AA1	√	-
145	6	Y3	W4	NA	-
146	6	U7	Y1	NA	-
147	6	V4	W1	√	-
148	6	U6	W2	√	VREF
149	6	T5	V3	√	-
150	6	U4	U5	√	-
151	6	U3	T7	NA	-

Table 4: **FG676 Fine-Pitch BGA Differential Pin Pair Summary — XCV405E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
152	6	T6	U2	NA	-
153	6	T4	U1	NA	-
154	6	T3	R7	NA	-
155	6	R6	R4	√	VREF
156	6	R5	R3	√	-
157	6	P7	P8	NA	-
158	6	P6	R1	NA	VREF
159	6	P4	P5	√	-
160	7	N8	N5	√	-
161	7	N3	N6	√	-
162	7	M2	N4	NA	VREF
163	7	M7	N7	NA	-
164	7	M3	M6	√	-
165	7	M5	M4	√	VREF
166	7	L7	L3	NA	-
167	7	K2	L6	NA	-
168	7	K1	L4	NA	-
169	7	L5	K3	NA	-
170	7	J3	K5	√	-
171	7	J4	K4	√	-
172	7	K6	H3	√	VREF
173	7	G3	K7	√	-
174	7	H1	J5	NA	-
175	7	J6	G2	NA	-
176	7	F1	J7	√	-
177	7	G4	H4	√	VREF
178	7	H5	F3	NA	-
179	7	H6	E2	NA	-
180	7	F4	G5	NA	VREF
181	7	G6	H7	NA	-
182	7	E4	E3	√	-

FG900 Fine-Pitch Ball Grid Array Package

The XCV812E Virtex-E Extended Memory devices are available in the FG900 fine-pitch BGA package. Pins labeled I0_VREF can be used as either. If the pin is not used as V_{REF}, it can be used as general I/O. Immediately following Table 5, see Table 6 for FG900 package Differential Pair information.

Table 5: **FG900 Fine-Pitch BGA Package — XCV812E**

Bank	Description	Pin
0	GCK3	C15
0	IO	A7
0	IO	A13
0	IO	C9
0	IO	C10
0	IO	D10
0	IO	E6
0	IO	F7
0	IO	F9
0	IO	F15
0	IO	G12
0	IO	G15
0	IO	H15
0	IO	J10
0	IO	K12
0	IO_VREF	A9
0	IO_L1N_Y	D5
0	IO_L1P_Y	G8
0	IO_L2N_Y	A3
0	IO_L2P_Y	H9
0	IO_L4N_YY	A4
0	IO_L4P_YY	D6
0	IO_VREF_L5N_YY	E7
0	IO_L5P_YY	B5
0	IO_L6N	A5
0	IO_L6P	F8
0	IO_L7N	D7
0	IO_L7P	N11

Table 5: **FG900 Fine-Pitch BGA Package — XCV812E**

Bank	Description	Pin
0	IO_L8N_YY	G9
0	IO_L8P_YY	E8
0	IO_VREF_L9N_YY	A6
0	IO_L9P_YY	J11
0	IO_L10N	C7
0	IO_L10P	B7
0	IO_L11N	C8
0	IO_L11P	H10
0	IO_L12N_YY	G10
0	IO_L12P_YY	F10
0	IO_VREF_L13N_YY	A8
0	IO_L13P_YY	H11
0	IO_L15N	B9
0	IO_L15P	J12
0	IO_L17N	G11
0	IO_L17P	B10
0	IO_L19N_Y	H13
0	IO_L19P_Y	F11
0	IO_L20N_Y	E11
0	IO_L20P_Y	D11
0	IO_L22N_YY	F12
0	IO_L22P_YY	C11
0	IO_VREF_L23N_YY	A10
0	IO_L23P_YY	D12
0	IO_L24N	E12
0	IO_L24P	A11
0	IO_L25N	G13
0	IO_L25P	B12
0	IO_L26N_YY	A12
0	IO_L26P_YY	K13
0	IO_VREF_L27N_YY	F13
0	IO_L27P_YY	B13
0	IO_L28N	G14
0	IO_L28P	E13

Table 5: **FG900 Fine-Pitch BGA Package — XCV812E**

Bank	Description	Pin
0	IO_L29N	D14
0	IO_L29P	B14
0	IO_L30N_YY	A14
0	IO_L30P_YY	J14
0	IO_VREF_L31N_YY	K14
0	IO_L31P_YY	J15
0	IO_LVDS_DLL_L34N	A15
1	GCk2	E15
1	IO	B18
1	IO	B21
1	IO	B28
1	IO	C23
1	IO	C26
1	IO	D20
1	IO	D23
1	IO_LVDS_DLL_L34P	E16
1	IO_L35N	B16
1	IO_L35P	F16
1	IO_L36N	A16
1	IO_L36P	H16
1	IO_L37N_YY	C16
1	IO_VREF_L37P_YY	K15
1	IO_L38N_YY	K16
1	IO_L38P_YY	G16
1	IO_L39N	A17
1	IO_L39P	E17
1	IO_L40N	F17
1	IO_L40P	C17
1	IO_L41N_YY	E18
1	IO_VREF_L41P_YY	A18
1	IO_L42N_YY	D18
1	IO_L42P_YY	A19
1	IO_L43N	B19

Table 5: **FG900 Fine-Pitch BGA Package — XCV812E**

Bank	Description	Pin
1	IO_L43P	G18
1	IO_L44N	D19
1	IO_L44P	H18
1	IO_L45N_YY	F18
1	IO_VREF_L45P_YY	F19
1	IO_L46N_YY	B20
1	IO_L46P_YY	K17
1	IO_L48N_Y	G19
1	IO_L48P_Y	C20
1	IO_L49N_Y	K18
1	IO_L49P_Y	E20
1	IO_L51N_YY	F20
1	IO_L51P_YY	A21
1	IO_L52N_YY	C21
1	IO_VREF_L52P_YY	A22
1	IO_L53N	H19
1	IO_L53P	B22
1	IO_L54N	E21
1	IO_L54P	D22
1	IO_L55N_YY	F21
1	IO_VREF_L55P_YY	C22
1	IO_L56N_YY	H20
1	IO_L56P_YY	E22
1	IO_L57N	G21
1	IO_L57P	A23
1	IO_L58N	A24
1	IO_L58P	K19
1	IO_L59N_YY	C24
1	IO_VREF_L59P_YY	B24
1	IO_L60N_YY	H21
1	IO_L60P_YY	G22
1	IO_L61N	E23
1	IO_L61P	C25
1	IO_L62N	D24

Table 5: **FG900 Fine-Pitch BGA Package — XCV812E**

Bank	Description	Pin
1	IO_L62P	A26
1	IO_L63N_YY	B26
1	IO_VREF_L63P_YY	K20
1	IO_L64N_YY	D25
1	IO_L64P_YY	J21
1	IO_L66N_Y	B27
1	IO_L66P_Y	G23
1	IO_L67N_Y	A27
1	IO_L67P_Y	F24
1	IO_WRITE_L69N_YY	K21
1	IO_CS_L69P_YY	C27
2	IO	D28
2	IO	F27
2	IO	H25
2	IO	J25
2	IO	J28
2	IO	K28
2	IO	K30
2	IO	M23
2	IO	N20
2	IO	N23
2	IO	R27
2	IO	R28
2	IO	R30
2	IO_DOUT_BUSY_L70P_YY	J22
2	IO_DIN_D0_L70N_YY	E27
2	IO_L72P_Y	G25
2	IO_L72N_Y	E25
2	IO_L73P	E28
2	IO_L73N	C30
2	IO_L75P	D30
2	IO_L75N	J23
2	IO_VREF_L76P_Y	L21

Table 5: **FG900 Fine-Pitch BGA Package — XCV812E**

Bank	Description	Pin
2	IO_L76N_Y	F28
2	IO_L77P_YY	G28
2	IO_L77N_YY	E30
2	IO_L78P	G27
2	IO_L78N	E29
2	IO_L79P	K23
2	IO_L79N	H26
2	IO_VREF_L80P_YY	F30
2	IO_L80N_YY	L22
2	IO_L81P_YY	H27
2	IO_L81N_YY	G29
2	IO_L82P_Y	G30
2	IO_L82N_Y	M21
2	IO_L83P	J24
2	IO_L83N	J26
2	IO_VREF_L84P	H30
2	IO_L84N	L23
2	IO_L86P	J29
2	IO_L86N	K24
2	IO_VREF	J30
2	IO_D1_L88P	M22
2	IO_D2_L88N	K29
2	IO_L90P_Y	N21
2	IO_L90N_Y	K25
2	IO_L91P	L24
2	IO_L91N	L27
2	IO_L93P	L26
2	IO_L93N	L28
2	IO_VREF_L94P_Y	L30
2	IO_L94N_Y	M27
2	IO_L95P_YY	M26
2	IO_L95N_YY	M29
2	IO_L96P	N29
2	IO_L96N	M30

Table 5: **FG900 Fine-Pitch BGA Package — XCV812E**

Bank	Description	Pin
2	IO_L97P	N25
2	IO_L97N	N27
2	IO_VREF_L98P_YY	N30
2	IO_D3_L98N_YY	P21
2	IO_L99P_YY	N26
2	IO_L99N_YY	P28
2	IO_L100P_Y	P29
2	IO_L100N_Y	N24
2	IO_L101P	P22
2	IO_L101N	R26
2	IO_VREF_2_L102P	P25
2	IO_L102N	R29
2	IO_L104P	R25
2	IO_L104N	T30
2	IO_L106P	R24
3	IO	T24
3	IO	V24
3	IO	Y21
3	IO	Y27
3	IO	AB27
3	IO	AF28
3	IO	AG30
3	IO_L106N	U29
3	IO_L107P	R22
3	IO_L107N	T27
3	IO_L108P	R23
3	IO_L108N	T28
3	IO_L109P	T21
3	IO_VREF_L109N	T25
3	IO_L110P	U28
3	IO_L110N	U30
3	IO_L111P_Y	T23
3	IO_L111N_Y	U27

Table 5: **FG900 Fine-Pitch BGA Package — XCV812E**

Bank	Description	Pin
3	IO_L112P_YY	U25
3	IO_L112N_YY	V27
3	IO_D4_L113P_YY	U24
3	IO_VREF_L113N_YY	V29
3	IO_L114P	W30
3	IO_L114N	U22
3	IO_L115P	U21
3	IO_L115N	W29
3	IO_L116P_YY	V26
3	IO_L116N_YY	W27
3	IO_L117P_Y	W26
3	IO_VREF_L117N_Y	Y29
3	IO_L118P	W25
3	IO_L118N	Y30
3	IO_L120P	AA30
3	IO_L120N	W24
3	IO_L121P_Y	AA29
3	IO_L121N_Y	V20
3	IO_L123P_YY	Y26
3	IO_D5_L123N_YY	AB30
3	IO_D6_L124P_YY	V21
3	IO_VREF_L124N_YY	AA28
3	IO_L125P	Y25
3	IO_L125N	AA27
3	IO_L126P	W22
3	IO_L126N	Y23
3	IO_L127P	Y24
3	IO_VREF_L127N	AB28
3	IO_L128P	AC30
3	IO_L128N	AA25
3	IO_L129P_Y	W21
3	IO_L129N_Y	AA24
3	IO_L130P_YY	AB26
3	IO_L130N_YY	AD30

Table 5: **FG900 Fine-Pitch BGA Package — XCV812E**

Bank	Description	Pin
3	IO_L131P_YY	Y22
3	IO_VREF_L131N_YY	AC27
3	IO_L132P	AD28
3	IO_L132N	AB25
3	IO_L133P	AC26
3	IO_L133N	AE30
3	IO_L134P_YY	AD27
3	IO_L134N_YY	AF30
3	IO_L135P_Y	AF29
3	IO_VREF_L135N_Y	AB24
3	IO_L136P	AB23
3	IO_L136N	AE28
3	IO_L138P	AE26
3	IO_L138N	AG29
3	IO_L139P_Y	AH30
3	IO_L139N_Y	AC24
3	IO_D7_L141P_YY	AH29
3	IO_INIT_L141N_YY	AA22
4	GCK0	AJ16
4	IO	AB19
4	IO	AC16
4	IO	AC19
4	IO	AD19
4	IO	AD20
4	IO	AE21
4	IO	AF19
4	IO	AH17
4	IO	AH23
4	IO	AH26
4	IO	AH27
4	IO	AK18
4	IO_VREF_4	AA18
4	IO_L142P_YY	AF27

Table 5: **FG900 Fine-Pitch BGA Package — XCV812E**

Bank	Description	Pin
4	IO_L142N_YY	AK28
4	IO_L144P_Y	AD23
4	IO_L144N_Y	AJ27
4	IO_L145P_Y	AB21
4	IO_L145N_Y	AF25
4	IO_L147P_YY	AA21
4	IO_L147N_YY	AG25
4	IO_VREF_4_L148P_YY	AJ26
4	IO_L148N_YY	AD22
4	IO_L149P	AA20
4	IO_L149N	AH25
4	IO_L150P	AC21
4	IO_L150N	AF24
4	IO_L151P_YY	AG24
4	IO_L151N_YY	AK26
4	IO_VREF_4_L152P_YY	AJ24
4	IO_L152N_YY	AF23
4	IO_L153P	AE23
4	IO_L153N	AB20
4	IO_L154P	AC20
4	IO_L154N	AG23
4	IO_L155P_YY	AF22
4	IO_L155N_YY	AE22
4	IO_VREF_4_L156P_YY	AJ22
4	IO_L156N_YY	AG22
4	IO_L158P	AA19
4	IO_L158N	AF21
4	IO_L160P	AG21
4	IO_L160N	AK23
4	IO_L162P_Y	AE20
4	IO_L162N_Y	AJ21
4	IO_L163P_Y	AG20
4	IO_L163N_Y	AF20
4	IO_L165P_YY	AJ20

Table 5: **FG900 Fine-Pitch BGA Package — XCV812E**

Bank	Description	Pin
4	IO_L165N_YY	AE19
4	IO_VREF_4_L166P_YY	AK22
4	IO_L166N_YY	AH20
4	IO_L167P	AG19
4	IO_L167N	AB17
4	IO_L168P	AJ19
4	IO_L168N	AD17
4	IO_L169P_YY	AA16
4	IO_L169N_YY	AA17
4	IO_VREF_4_L170P_YY	AK21
4	IO_L170N_YY	AB16
4	IO_L171P	AG18
4	IO_L171N	AK20
4	IO_L172P	AK19
4	IO_L172N	AD16
4	IO_L173P_YY	AE16
4	IO_L173N_YY	AE17
4	IO_VREF_4_L174P_YY	AG17
4	IO_L174N_YY	AJ17
4	IO_L176P	AG16
4	IO_L176N	AK17
4	IO_LVDS_DLL_L177P	AF16
5	GCK1	AK16
5	IO	AD8
5	IO	AD14
5	IO	AE10
5	IO	AE12
5	IO	AG15
5	IO	AH5
5	IO	AH8
5	IO	AK12
5	IO_LVDS_DLL_L177N	AH16
5	IO_L179P	AB15

Table 5: **FG900 Fine-Pitch BGA Package — XCV812E**

Bank	Description	Pin
5	IO_L179N	AF15
5	IO_L180P_YY	AA15
5	IO_VREF_5_L180N_YY	AF14
5	IO_L181P_YY	AH15
5	IO_L181N_YY	AK15
5	IO_L182P	AB14
5	IO_L182N	AF13
5	IO_L183P	AH14
5	IO_L183N	AJ14
5	IO_L184P_YY	AE14
5	IO_VREF_5_L184N_YY	AG13
5	IO_L185P_YY	AK13
5	IO_L185N_YY	AD13
5	IO_L186P	AE13
5	IO_L186N	AF12
5	IO_L187P	AC13
5	IO_L187N	AA13
5	IO_L188P_YY	AA12
5	IO_VREF_5_L188N_YY	AJ12
5	IO_L189P_YY	AB12
5	IO_L189N_YY	AE11
5	IO_L191P_Y	AG11
5	IO_L191N_Y	AF11
5	IO_L192P_Y	AH11
5	IO_L192N_Y	AJ11
5	IO_L194P_YY	AD12
5	IO_L194N_YY	AK11
5	IO_L195P_YY	AJ10
5	IO_VREF_5_L195N_YY	AC12
5	IO_L196P	AK10
5	IO_L196N	AD11
5	IO_L197P	AJ9
5	IO_L197N	AE9
5	IO_L198P_YY	AH10

Table 5: **FG900 Fine-Pitch BGA Package — XCV812E**

Bank	Description	Pin
5	IO_VREF_5_L198N_YY	AF9
5	IO_L199P_YY	AH9
5	IO_L199N_YY	AK9
5	IO_L200P	AF8
5	IO_L200N	AB11
5	IO_L201P	AC11
5	IO_L201N	AG8
5	IO_L202P_YY	AK8
5	IO_VREF_5_L202N_YY	AF7
5	IO_L203P_YY	AG7
5	IO_L203N_YY	AK7
5	IO_L204P	AJ7
5	IO_L204N	AD10
5	IO_L205P	AH6
5	IO_L205N	AC10
5	IO_L206P_YY	AD9
5	IO_VREF_5_L206N_YY	AG6
5	IO_L207P_YY	AB10
5	IO_L207N_YY	AJ5
5	IO_L209P_Y	AC9
5	IO_L209N_Y	AJ4
5	IO_L210P_Y	AG5
5	IO_L210N_Y	AK4
6	IO	T6
6	IO	U1
6	IO	U6
6	IO	V7
6	IO	V8
6	IO	W10
6	IO	Y10
6	IO	AA2
6	IO	AA4
6	IO	AD1

Table 5: **FG900 Fine-Pitch BGA Package — XCV812E**

Bank	Description	Pin
6	IO	AD6
6	IO	AG2
6	IO_L212N_YY	AF3
6	IO_L212P_YY	AC6
6	IO_L214N_Y	AB9
6	IO_L214P_Y	AE4
6	IO_L215N	AE3
6	IO_L215P	AH1
6	IO_L217N	AG1
6	IO_L217P	AA10
6	IO_VREF_L218N_Y	AA9
6	IO_L218P_Y	AD4
6	IO_L219N_YY	AD5
6	IO_L219P_YY	AD2
6	IO_L220N	AD3
6	IO_L220P	AF2
6	IO_L221N	AA8
6	IO_L221P	AA7
6	IO_VREF_L222N_YY	AF1
6	IO_L222P_YY	Y9
6	IO_L223N_YY	AB6
6	IO_L223P_YY	AC4
6	IO_L224N_Y	AE1
6	IO_L224P_Y	W8
6	IO_L225N	Y8
6	IO_L225P	AB4
6	IO_VREF_L226N	AB3
6	IO_L226P	W9
6	IO_L228N	AB1
6	IO_L228P	V10
6	IO_VREF	AC1
6	IO_L230N	V11
6	IO_L230P	AA3
6	IO_L232N_Y	W7

Table 5: **FG900 Fine-Pitch BGA Package — XCV812E**

Bank	Description	Pin
6	IO_L232P_Y	AA6
6	IO_L233N	Y6
6	IO_L233P	Y4
6	IO_L235N	Y3
6	IO_L235P	Y2
6	IO_VREF_L236N_Y	Y5
6	IO_L236P_Y	W5
6	IO_L237N_YY	W4
6	IO_L237P_YY	W6
6	IO_L238N	V6
6	IO_L238P	W2
6	IO_L239N	U9
6	IO_L239P	V4
6	IO_VREF_L240N_YY	AB2
6	IO_L240P_YY	T8
6	IO_L241N_YY	U5
6	IO_L241P_YY	W1
6	IO_L242N_Y	Y1
6	IO_L242P_Y	T9
6	IO_L243N	T7
6	IO_L243P	U3
6	IO_VREF_L244N	T5
6	IO_L244P	V2
6	IO_L246N	T4
6	IO_L246P	U2
6	IO_L247N	T1
7	IO	D1
7	IO	E3
7	IO	J4
7	IO	J6
7	IO	K10
7	IO	L3
7	IO	M7

Table 5: **FG900 Fine-Pitch BGA Package — XCV812E**

Bank	Description	Pin
7	IO	N8
7	IO	R5
7	IO_L247P	R10
7	IO_L249N	R8
7	IO_L249P	R4
7	IO_L250N	R7
7	IO_L250P	R3
7	IO_L251N	P10
7	IO_VREF_L251P	P6
7	IO_L252N	P5
7	IO_L252P	P2
7	IO_L253N_Y	P7
7	IO_L253P_Y	P4
7	IO_L254N_YY	N4
7	IO_L254P_YY	R2
7	IO_L255N_YY	N7
7	IO_VREF_L255P_YY	P1
7	IO_L256N	M6
7	IO_L256P	N6
7	IO_L257N	N5
7	IO_L257P	N1
7	IO_L258N_YY	M4
7	IO_L258P_YY	M5
7	IO_L259N_Y	M2
7	IO_VREF_L259P_Y	M1
7	IO_L260N	L4
7	IO_L260P	L2
7	IO_L262N	L1
7	IO_L262P	M8
7	IO_L263N_Y	K2
7	IO_L263P_Y	M9
7	IO_L265N_YY	K5
7	IO_L265P_YY	K1
7	IO_L266N_YY	L6

Table 5: **FG900 Fine-Pitch BGA Package — XCV812E**

Bank	Description	Pin
7	IO_VREF_L266P_YY	K3
7	IO_L267N	L7
7	IO_L267P	K4
7	IO_L268N	L8
7	IO_L268P	J5
7	IO_L269N	K6
7	IO_VREF_L269P	H4
7	IO_L270N	H1
7	IO_L270P	K7
7	IO_L271N_Y	J7
7	IO_L271P_Y	J2
7	IO_L272N_YY	H5
7	IO_L272P_YY	G2
7	IO_L273N_YY	L9
7	IO_VREF_L273P_YY	G5
7	IO_L274N	F3
7	IO_L274P	K8
7	IO_L275N	G3
7	IO_L275P	E1
7	IO_L276N_YY	H6
7	IO_L276P_YY	E2
7	IO_L277N_Y	E4
7	IO_VREF_L277P_Y	K9
7	IO_L278N	J8
7	IO_L278P	F4
7	IO_L280N	G6
7	IO_L280P	C2
7	IO_L281N_Y	D2
7	IO_L281P_Y	F5
2	DONE	AJ28
NA	DXN	AJ3
NA	DXP	AH4
3	CCLK	F26

Table 5: **FG900 Fine-Pitch BGA Package — XCV812E**

Bank	Description	Pin
NA	M0	AF4
NA	M1	AC7
NA	M2	AK3
NA	PROGRAM	AG28
NA	TCK	B3
NA	TDI	H22
2	TDO	D26
NA	TMS	C1
NA	VCCINT	L11
NA	VCCINT	L12
NA	VCCINT	L19
NA	VCCINT	L20
NA	VCCINT	M11
NA	VCCINT	M12
NA	VCCINT	M19
NA	VCCINT	M20
NA	VCCINT	N13
NA	VCCINT	N14
NA	VCCINT	N15
NA	VCCINT	N16
NA	VCCINT	N17
NA	VCCINT	N18
NA	VCCINT	P13
NA	VCCINT	P18
NA	VCCINT	R13
NA	VCCINT	R18
NA	VCCINT	T13
NA	VCCINT	T18
NA	VCCINT	U18
NA	VCCINT	U13
NA	VCCINT	V13
NA	VCCINT	V14
NA	VCCINT	V15

Table 5: **FG900 Fine-Pitch BGA Package — XCV812E**

Bank	Description	Pin
NA	VCCINT	V16
NA	VCCINT	V17
NA	VCCINT	V18
NA	VCCINT	W11
NA	VCCINT	W12
NA	VCCINT	W19
NA	VCCINT	W20
NA	VCCINT	Y11
NA	VCCINT	Y12
NA	VCCINT	Y19
NA	VCCINT	Y20
NA	VCCO_0	B6
NA	VCCO_0	M15
NA	VCCO_0	M14
NA	VCCO_0	L15
NA	VCCO_0	L14
NA	VCCO_0	H14
NA	VCCO_0	M13
NA	VCCO_0	C12
NA	VCCO_1	B25
NA	VCCO_1	C19
NA	VCCO_1	M18
NA	VCCO_1	M17
NA	VCCO_1	L17
NA	VCCO_1	H17
NA	VCCO_1	L16
NA	VCCO_1	M16
NA	VCCO_2	F29
NA	VCCO_2	M28
NA	VCCO_2	P23
NA	VCCO_2	R20
NA	VCCO_2	P20
NA	VCCO_2	R19

Table 5: **FG900 Fine-Pitch BGA Package — XCV812E**

Bank	Description	Pin
NA	VCCO_2	N19
NA	VCCO_2	P19
NA	VCCO_3	AE29
NA	VCCO_3	W28
NA	VCCO_3	U23
NA	VCCO_3	U20
NA	VCCO_3	T20
NA	VCCO_3	V19
NA	VCCO_3	T19
NA	VCCO_3	U19
NA	VCCO_4	AJ25
NA	VCCO_4	AH19
NA	VCCO_4	W18
NA	VCCO_4	AC17
NA	VCCO_4	Y17
NA	VCCO_4	W17
NA	VCCO_4	W16
NA	VCCO_4	Y16
NA	VCCO_5	AJ6
NA	VCCO_5	Y15
NA	VCCO_5	W15
NA	VCCO_5	AC14
NA	VCCO_5	Y14
NA	VCCO_5	W14
NA	VCCO_5	W13
NA	VCCO_5	AH12
NA	VCCO_6	AE2
NA	VCCO_6	V12
NA	VCCO_6	U12
NA	VCCO_6	T12
NA	VCCO_6	U11
NA	VCCO_6	T11
NA	VCCO_6	U8
NA	VCCO_6	W3

Table 5: **FG900 Fine-Pitch BGA Package — XCV812E**

Bank	Description	Pin
NA	VCCO_7	F2
NA	VCCO_7	R12
NA	VCCO_7	P12
NA	VCCO_7	N12
NA	VCCO_7	R11
NA	VCCO_7	P11
NA	VCCO_7	P8
NA	VCCO_7	M3
NA	GND	Y18
NA	GND	AH7
NA	GND	AK30
NA	GND	AJ30
NA	GND	B30
NA	GND	A30
NA	GND	AK29
NA	GND	AJ29
NA	GND	AC29
NA	GND	H29
NA	GND	B29
NA	GND	A29
NA	GND	AH28
NA	GND	V28
NA	GND	N28
NA	GND	C28
NA	GND	AG27
NA	GND	D27
NA	GND	AF26
NA	GND	E26
NA	GND	F25
NA	GND	AE25
NA	GND	G24
NA	GND	AJ23
NA	GND	AD24

Table 5: **FG900 Fine-Pitch BGA Package — XCV812E**

Bank	Description	Pin
NA	GND	H23
NA	GND	B23
NA	GND	AC23
NA	GND	AB22
NA	GND	V22
NA	GND	N22
NA	GND	AH18
NA	GND	AB18
NA	GND	J18
NA	GND	C18
NA	GND	U17
NA	GND	T17
NA	GND	R17
NA	GND	P17
NA	GND	U16
NA	GND	T16
NA	GND	R16
NA	GND	P16
NA	GND	U15
NA	GND	T15
NA	GND	R15
NA	GND	P15
NA	GND	U14
NA	GND	T14
NA	GND	R14
NA	GND	P14
NA	GND	AH13
NA	GND	AB13
NA	GND	J13
NA	GND	C13
NA	GND	V9
NA	GND	N9
NA	GND	J9
NA	GND	AJ8

Table 5: **FG900 Fine-Pitch BGA Package — XCV812E**

Bank	Description	Pin
NA	GND	AC8
NA	GND	H8
NA	GND	AD7
NA	GND	B8
NA	GND	AE6
NA	GND	G7
NA	GND	F6
NA	GND	AF5
NA	GND	E5
NA	GND	AG4
NA	GND	D4
NA	GND	V3
NA	GND	N3
NA	GND	C3
NA	GND	AK2
NA	GND	AH3
NA	GND	AC2
NA	GND	H2
NA	GND	B2
NA	GND	A2
NA	GND	AK1
NA	GND	AJ2
NA	GND	AJ1
NA	GND	A1
NA	GND	B1

FG900 Differential Pin Pairs

Virtex-E Extended Memory devices have differential pin pairs that can also provide other functions when not used as a differential pair. A √ in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package.

Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair is in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs that can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock.

Table 6: **FG900 Differential Pin Pair Summary — XCV812E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
GCLK LVDS					
3	0	C15	A15	NA	IO LVDS 34
2	1	E15	E16	NA	IO LVDS 34
1	5	AK16	AH16	NA	IO LVDS 177
0	4	AJ16	AF16	NA	IO LVDS 177
IO LVDS Total Pairs: 235, Asynchronous Output Pairs: 85					
1	0	G8	D5	√	-
2	0	H9	A3	√	-
4	0	D6	A4	√	-
5	0	B5	E7	√	VREF
6	0	F8	A5	-	-
7	0	N11	D7	-	-
8	0	E8	G9	√	-
9	0	J11	A6	√	VREF
10	0	B7	C7	-	-
11	0	H10	C8	-	-
12	0	F10	G10	√	-
13	0	H11	A8	√	VREF
15	0	J12	B9	-	-
17	0	B10	G11	-	-
19	0	F11	H13	√	-
20	0	D11	E11	√	-
22	0	C11	F12	√	-
23	0	D12	A10	√	VREF
24	0	A11	E12	-	-

Table 6: **FG900 Differential Pin Pair Summary — XCV812E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
25	0	B12	G13	-	-
26	0	K13	A12	√	-
27	0	B13	F13	√	VREF
28	0	E13	G14	-	-
29	0	B14	D14	-	-
30	0	J14	A14	√	-
31	0	J15	K14	√	VREF
34	1	E16	A15	-	GCLK LVDS 3/2
35	1	F16	B16	-	-
36	1	H16	A16	-	-
37	1	K15	C16	√	VREF
38	1	G16	K16	√	-
39	1	E17	A17	-	-
40	1	C17	F17	-	-
41	1	A18	E18	√	VREF
42	1	A19	D18	√	-
43	1	G18	B19	-	-
44	1	H18	D19	-	-
45	1	F19	F18	√	VREF
46	1	K17	B20	√	-
48	1	C20	G19	√	-
49	1	E20	K18	√	-
51	1	A21	F20	√	-
52	1	A22	C21	√	VREF
53	1	B22	H19	-	-
54	1	D22	E21	-	-
55	1	C22	F21	√	VREF
56	1	E22	H20	√	-
57	1	A23	G21	-	-
58	1	K19	A24	-	-
59	1	B24	C24	√	VREF
60	1	G22	H21	√	-
61	1	C25	E23	-	-
62	1	A26	D24	-	-
63	1	K20	B26	√	VREF
64	1	J21	D25	√	-
66	1	G23	B27	√	-

Table 6: **FG900 Differential Pin Pair Summary — XCV812E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
67	1	F24	A27	√	-
69	1	C27	K21	√	CS
70	2	J22	E27	√	DIN_D0
72	2	G25	E25	√	-
73	2	E28	C30	-	-
75	2	D30	J23	-	-
76	2	L21	F28	√	VREF
77	2	G28	E30	√	-
78	2	G27	E29	-	-
79	2	K23	H26	-	-
80	2	F30	L22	√	VREF
81	2	H27	G29	√	-
82	2	G30	M21	√	-
83	2	J24	J26	-	-
84	2	H30	L23	-	VREF
86	2	J29	K24	-	-
88	2	M22	K29	-	D2
90	2	N21	K25	√	-
91	2	L24	L27	-	-
93	2	L26	L28	-	-
94	2	L30	M27	√	VREF
95	2	M26	M29	√	-
96	2	N29	M30	-	-
97	2	N25	N27	-	-
98	2	N30	P21	√	D3
99	2	N26	P28	√	-
100	2	P29	N24	√	-
101	2	P22	R26	-	-
102	2	P25	R29	-	VREF
104	2	R25	T30	-	-
106	3	R24	U29	-	TRDY
107	3	R22	T27	-	-
108	3	R23	T28	-	-
109	3	T21	T25	-	VREF
110	3	U28	U30	-	-
111	3	T23	U27	√	-
112	3	U25	V27	√	-

Table 6: **FG900 Differential Pin Pair Summary — XCV812E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
113	3	U24	V29	√	VREF
114	3	W30	U22	-	-
115	3	U21	W29	-	-
116	3	V26	W27	√	-
117	3	W26	Y29	√	VREF
118	3	W25	Y30	-	-
120	3	AA30	W24	-	-
121	3	AA29	V20	√	-
123	3	Y26	AB30	√	D5
124	3	V21	AA28	√	VREF
125	3	Y25	AA27	-	-
126	3	W22	Y23	-	-
127	3	Y24	AB28	-	VREF
128	3	AC30	AA25	-	-
129	3	W21	AA24	√	-
130	3	AB26	AD30	√	-
131	3	Y22	AC27	√	VREF
132	3	AD28	AB25	-	-
133	3	AC26	AE30	-	-
134	3	AD27	AF30	√	-
135	3	AF29	AB24	√	VREF
136	3	AB23	AE28	-	-
138	3	AE26	AG29	-	-
139	3	AH30	AC24	√	-
141	3	AH29	AA22	√	INIT
142	4	AF27	AK28	√	-
144	4	AD23	AJ27	√	-
145	4	AB21	AF25	√	-
147	4	AA21	AG25	√	-
148	4	AJ26	AD22	√	VREF
149	4	AA20	AH25	-	-
150	4	AC21	AF24	-	-
151	4	AG24	AK26	√	-
152	4	AJ24	AF23	√	VREF
153	4	AE23	AB20	-	-
154	4	AC20	AG23	-	-
155	4	AF22	AE22	√	-

Table 6: **FG900 Differential Pin Pair Summary — XCV812E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
156	4	AJ22	AG22	√	VREF
158	4	AA19	AF21	-	-
160	4	AG21	AK23	-	-
162	4	AE20	AJ21	√	-
163	4	AG20	AF20	√	-
165	4	AJ20	AE19	√	-
166	4	AK22	AH20	√	VREF
167	4	AG19	AB17	-	-
168	4	AJ19	AD17	-	-
169	4	AA16	AA17	√	-
170	4	AK21	AB16	√	VREF
171	4	AG18	AK20	-	-
172	4	AK19	AD16	-	-
173	4	AE16	AE17	√	-
174	4	AG17	AJ17	√	VREF
176	4	AG16	AK17	-	-
177	5	AF16	AH16	-	GCLK LVDS 1/0
179	5	AB15	AF15	-	-
180	5	AA15	AF14	√	VREF
181	5	AH15	AK15	√	-
182	5	AB14	AF13	-	-
183	5	AH14	AJ14	-	-
184	5	AE14	AG13	√	VREF
185	5	AK13	AD13	√	-
186	5	AE13	AF12	-	-
187	5	AC13	AA13	-	-
188	5	AA12	AJ12	√	VREF
189	5	AB12	AE11	√	-
191	5	AG11	AF11	√	-
192	5	AH11	AJ11	√	-
194	5	AD12	AK11	√	-
195	5	AJ10	AC12	√	VREF
196	5	AK10	AD11	-	-
197	5	AJ9	AE9	-	-
198	5	AH10	AF9	√	VREF
199	5	AH9	AK9	√	-
200	5	AF8	AB11	-	-

Table 6: **FG900 Differential Pin Pair Summary — XCV812E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
201	5	AC11	AG8	-	-
202	5	AK8	AF7	√	VREF
203	5	AG7	AK7	√	-
204	5	AJ7	AD10	-	-
205	5	AH6	AC10	-	-
206	5	AD9	AG6	√	VREF
207	5	AB10	AJ5	√	-
209	5	AC9	AJ4	√	-
210	5	AG5	AK4	√	-
212	6	AC6	AF3	√	-
214	6	AE4	AB9	√	-
215	6	AH1	AE3	-	-
217	6	AA10	AG1	-	-
218	6	AD4	AA9	√	VREF
219	6	AD2	AD5	√	-
220	6	AF2	AD3	-	-
221	6	AA7	AA8	-	-
222	6	Y9	AF1	√	VREF
223	6	AC4	AB6	√	-
224	6	W8	AE1	√	-
225	6	AB4	Y8	-	-
226	6	W9	AB3	-	VREF
228	6	V10	AB1	-	-
230	6	AA3	V11	-	-
232	6	AA6	W7	√	-
233	6	Y4	Y6	-	-
235	6	Y2	Y3	-	-
236	6	W5	Y5	√	VREF
237	6	W6	W4	√	-
238	6	W2	V6	-	-
239	6	V4	U9	-	-
240	6	T8	AB2	√	VREF
241	6	W1	U5	√	-
242	6	T9	Y1	√	-
243	6	U3	T7	-	-
244	6	V2	T5	-	VREF
246	6	U2	T4	-	-

Table 6: **FG900 Differential Pin Pair Summary — XCV812E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
247	7	R10	T1	-	IRDY
249	7	R4	R8	-	-
250	7	R3	R7	-	-
251	7	P6	P10	-	VREF
252	7	P2	P5	-	-
253	7	P4	P7	√	-
254	7	R2	N4	√	-
255	7	P1	N7	√	VREF
256	7	N6	M6	-	-
257	7	N1	N5	-	-
258	7	M5	M4	√	-
259	7	M1	M2	√	VREF
260	7	L2	L4	-	-
262	7	M8	L1	-	-
263	7	M9	K2	√	-
265	7	K1	K5	√	-
266	7	K3	L6	√	VREF
267	7	K4	L7	-	-
268	7	J5	L8	-	-
269	7	H4	K6	-	VREF
270	7	K7	H1	-	-
271	7	J2	J7	√	-
272	7	G2	H5	√	-
273	7	G5	L9	√	VREF
274	7	K8	F3	-	-
275	7	E1	G3	-	-
276	7	E2	H6	√	-
277	7	K9	E4	√	VREF
278	7	F4	J8	-	-
280	7	C2	G6	-	-
281	7	F5	D2	-	-

Virtex-E Extended Memory Device/Package Combinations and Maximum I/O

Virtex-E Extended Memory Series Maximum User I/O by Device/Package (Excluding Dedicated Clock Pins)		
Package	**XCV405E**	**XCV812E**
BG560	404	404
FG676	404	
FG900		556

Virtex-E Ordering Information

Virtex-II ordering information is shown in Figure 1

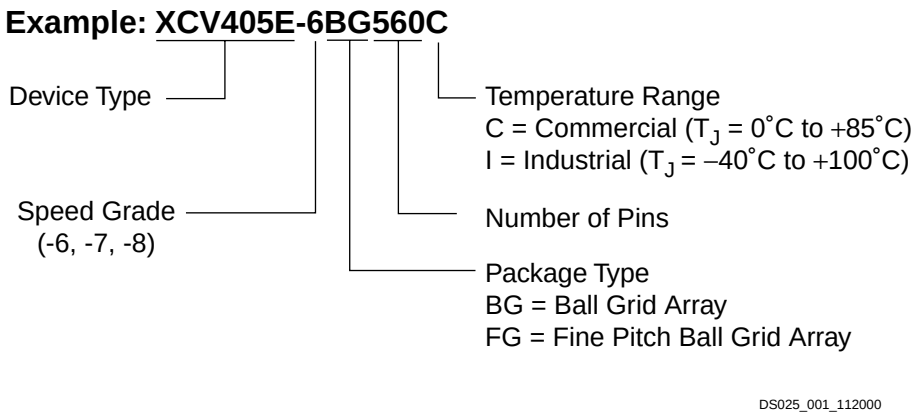

Figure 1: **Virtex Ordering Information**

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/23/00	1.0	Initial Xilinx release.
08/01/00	1.1	Accumulated edits and fixes. Upgrade to Preliminary. Preview -8 numbers added. Reformatted to adhere to corporate documentation style guidelines. Minor changes in BG560 pin-out table.
09/19/00	1.2	• In Table 3 (Module 4), **FG676 Fine-Pitch BGA — XCV405E**, the following pins are no longer labeled as VREF: B7, G16, G26, W26, AF20, AF8, Y1, H1. • Min values added to **Virtex-E Electrical Characteristics** tables.
11/20/00	1.3	• Updated speed grade -8 numbers in **Virtex-E Electrical Characteristics** tables (Module 3). • Updated minimums in Table 11 (Module 2), and added notes to Table 12 (Module 2). • Added to note 2 of **Absolute Maximum Ratings** (Module 3). • Changed all minimum hold times to –0.4 for **Global Clock Set-Up and Hold for LVTTL Standard, with DLL** (Module 3). • Revised maximum T_{DLLPW} in -6 speed grade for **DLL Timing Parameters** (Module 3).
04/02/01	1.4	• In Table 4, **FG676 Fine-Pitch BGA — XCV405E**, pin B19 is no longer labeled as VREF, and pin G16 is now labeled as VREF. • Updated values in Virtex-E Switching Characteristics tables. • Converted data sheet to modularized format. See the Virtex-E Extended Memory Data Sheet section.
07/23/01	1.5	• Changed definition of T31 and T32 pins in Table 1 for XCV405E and the XCV812E devices.

Virtex-E Extended Memory Data Sheet

The Virtex-E Extended Memory Data Sheet contains the following modules:

- DS025-1, Virtex-E 1.8V Extended Memory FPGAs: **Introduction and Ordering Information (Module 1)**
- DS025-2, Virtex-E 1.8V Extended Memory FPGAs: **Functional Description (Module 2)**
- DS025-3, Virtex-E 1.8V Extended Memory FPGAs: **DC and Switching Characteristics (Module 3)**
- DS025-4, Virtex-E 1.8V Extended Memory FPGAs: **Pinout Tables (Module 4)**