

Summary of Features

- System-level, high-capacity, pre-configured solution for Virtex® and Spartan® FPGAs
- Industry standard Flash memory combined with Xilinx controller technology
- Effortless density migration from 16 Megabits (Mb) to 64 Mb
- V_{CC} I/O: 1.8V, 2.5V, and 3.3V
- Configuration rates up to 152 Mb per second (Mb/s)
- Flexible configuration solution
 - Slave-SelectMAP
 - Slave-Serial
 - Concurrent Slave-Serial (up to eight separate chains)
- Patented compression technology (up to 2x compression)
- JTAG interface allows:
 - Access to the standard Flash memory
 - Boundary scan testing
- Native interface to the Flash memory is accessible for:
 - In-system parallel programming
 - Processor access to unused Flash memory locations
- Supports up to eight separate design sets (selectable by mode pins or via JTAG) enabling systems to reconfigure FPGAs for different functions
- Compatibility with IEEE Standard 1532
- User-friendly software to format and program the bitstreams into the standard Flash via the patented Flash programming engine
- Internet Reconfigurable Logic (IRL) upgradable system

Description

The System ACE™ Soft Controller (SC) solution addresses the need for a space-efficient, pre-engineered, high-density configuration solution in multiple FPGA systems. System ACE technology is a ground-breaking in-system programmable configuration solution that provides substantial savings in development effort and cost per bit over traditional PROM and embedded solutions for high capacity FPGA systems.

The System ACE SC solution is identical, in terms of features and functionality, to the System ACE MPM solution. At power-up, the System ACE SC (XCV50E-6CS144) controller reads the bitstream data from an AMD Flash memory unit and delivers the bitstream data to one or more target FPGAs using the Slave-Serial or SelectMAP FPGA configuration protocols. The target FPGAs may be reconfigured at anytime with one of the eight possible user design sets. The System ACE SC supports in-system reprogramming of the Flash memory unit.

Whereas, the System ACE MPM solution pre-packages the Flash memory unit and the Virtex-E-based configuration controller in a single BG388 package, the System ACE SC provides the freedom to select and place the individual components as desired on the board. The System ACE SC solution offers the System ACE MPM configuration controller technology as a pre-designed bitstream in the form of an MCS file.

The System ACE SC controller has four major interfaces. (See [Figure 1](#).) The Boundary Scan JTAG interface is provided for Boundary Scan test and Boundary Scan-based Flash memory programming. The system control interface provides an input for the system clock, design set selection pins, system configuration control signals, and system configuration status signals. The Flash memory interface connects to the external Flash memory unit for reading stored FPGA bitstream data and for reprogramming the Flash memory in-system. The target FPGA interface provides the signals to configure target FPGAs via the Slave-Serial, concurrent Slave-Serial, or SelectMAP configuration modes.

Separate power pins provide voltage compatibility control for the target FPGA configuration interface and for the system control/status interface.

Refer to the *System ACE MPM* data sheet (DS087) for descriptions of the System ACE MPM configuration model, System ACE MPM configuration performance, System ACE software, and Flash memory programming support. Differences between the System ACE SC and System ACE MPM are noted in the *System ACE SC and System ACE MPM Differences* section.

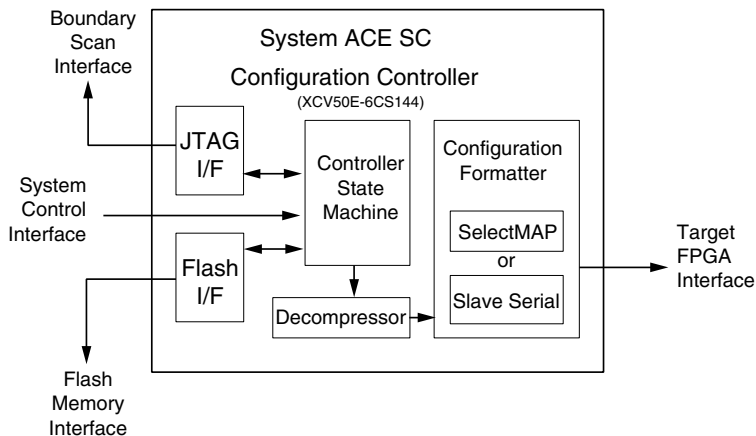


Figure 1: System ACE SC Interfaces

System ACE SC Solution Components

The complete System ACE SC solution is comprised of the Virtex-E (XCV50E-6CS144) configuration controller, the XC17V01 configuration PROM, the AMD Flash memory unit, and a few passive components. See Figure 2 for a complete view of the components and schematic of the signals between the System ACE SC components.

Specific pin information is described in the *Pinout and Pin Descriptions* section.

XCV50E-6CS144 Configuration Controller

The System ACE SC configuration controller design is available for a Virtex-E (XCV50E-6CS144) FPGA (Table 1).

Table 1: Configuration Controller Device Information

Device Type	Speed Grade	Package
XCV50E	-6	CS144

Notes:
 1. The System ACE SC configuration controller design is available for only the CS144 package.

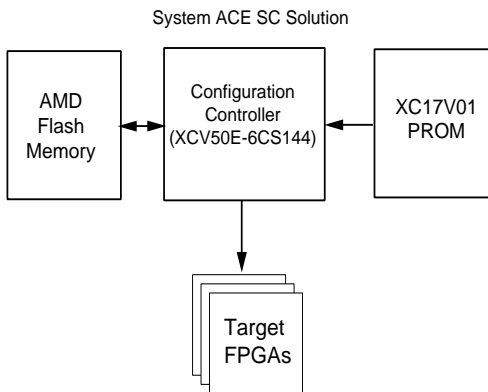


Figure 2: System ACE SC Components

Specific information for the XCV50E is available in the Virtex-E FPGA Family data sheets (Table 2).

Table 2: Virtex-E Data Sheets

Description	Location
Virtex-E Introduction and Ordering Information	http://www.xilinx.com/partinfo/ds022-1.pdf
Virtex-E Detailed Functional Description	http://www.xilinx.com/partinfo/ds022-2.pdf
Virtex-E DC and Switching Characteristics	http://www.xilinx.com/partinfo/ds022-3.pdf
Virtex-E Pinout Tables	http://www.xilinx.com/partinfo/ds022-4.pdf

XC17V01 Configuration PROM

The System ACE SC configuration controller design is available in an Intel Extended Hexadecimal Format (Xilinx MCS extension) file format. The controller design is stored in an XC17V01 PROM. At power-up, the XC17V01 PROM configures the XCV50E-6CS144 FPGA with the System ACE SC configuration controller design.

Specific information for the XC17V01 PROM is available in the XC17V00 Series Configuration PROM data sheet at:

<http://www.xilinx.com/partinfo/ds073.pdf>

AMD Flash Memory

The System ACE SC stores target FPGA bitstream data in AMD Flash memory. Flash memory densities up to 64 Mb are supported. See [Table 3](#).

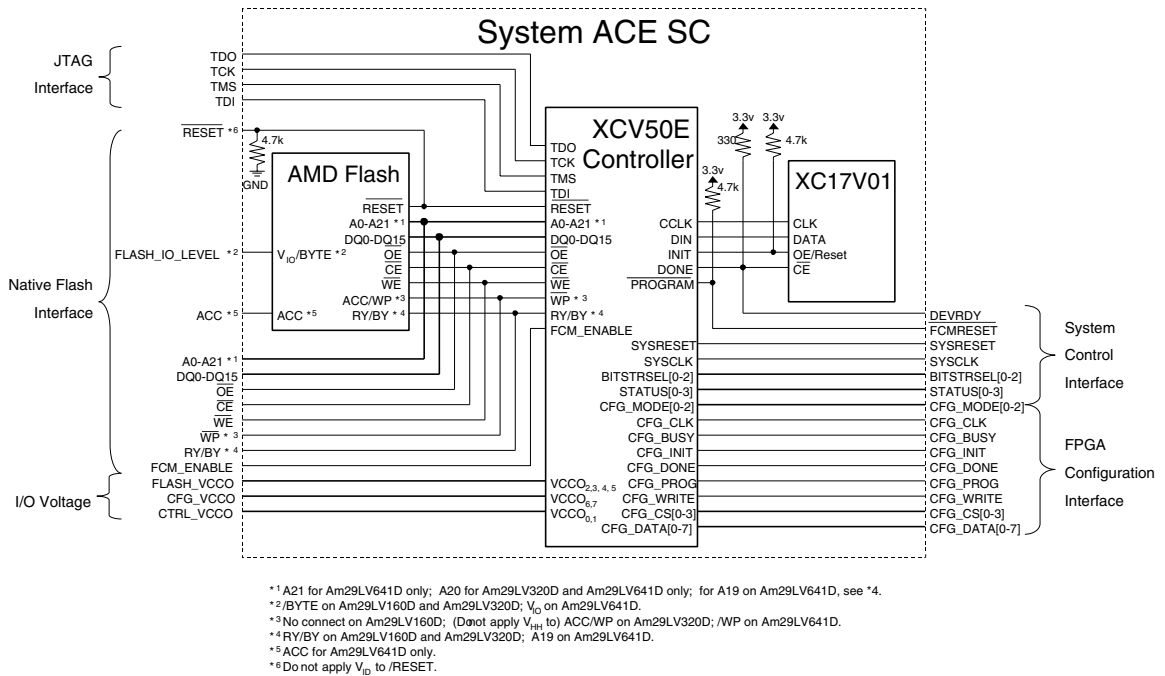
See the AMD Flash memory data sheets for additional information.

Table 3: Supported AMD Flash Memory Device Product Numbers

Flash Device Product Number	Flash Density	Flash Speed Grade	Flash Organization
AMD Am29LV160DT-90 AMD Am29LV160DB-90	16 Mb	90 ns	1M x 16-bit (or 2M x 8-bit)
AMD AM29LV320DT90 AMD AM29LV320DB90	32 Mb	90 ns	2M x 16-bit (or 4M x 8-bit)
AMD AM29LV641DH90R AMD AM29LV641DL90R	64 Mb	90 ns	4M x 16-bit

Pinout and Pin Descriptions

The components of the System ACE SC solution are connected as shown in **Figure 3**. Specific pin information is shown in the tables below. Separate power pins provide voltage compatibility control for the target FPGA configuration interface and for the system control/status interface.



ds088_03_091701

Figure 3: System ACE SC Schematic

XCV50E Control and Status Pins

Table 4 provides the control and status pins.

Table 4: XCV50E Control and Status Pins

CS144	Pin Name	Type	Description
A4	FCM_ENABLE	Input	Enables the System ACE flash controller module. Set FCM_ENABLE low to disable flash control signals and allow an external device to access the Flash memory.
A6	SYSCLK	Input	Controller system clock (maximum frequency = 133 MHz).
A5	SYSRESET	Input	Controller system reset. When pulsed High, SYSRESET resets the target FPGAs, samples the BITSTRSEL[2:0] pins, and downloads the corresponding data set.
B4	BITSTRSEL[0]	Input	Data set select bit 0.
B3	BITSTRSEL[1]	Input	Data set select bit 1.
A3	BITSTRSEL[2]	Input	Data set select bit 2.
D6	STATUS[0]	Output	Status bit 0.
C6	STATUS[1]	Output	Status bit 1.

Table 4: XCV50E Control and Status Pins (Continued)

CS144	Pin Name	Type	Description
C4	STATUS[2]	Output	Status bit 2.
B5	STATUS[3]	Output	Status bit 3.

Notes:
 1. XCV50E pins not listed in the tables below are no connects.

XCV50E Configuration Pins for Target FPGAs

Table 5 provides the configuration pins for target FPGAs.

Table 5: XCV50E Configuration Pins for Target FPGAs

CS144	Pin Name	Type	Description
F4	CFG_MODE[0]	Output	FPGA configuration mode control signal, M0.
F3	CFG_MODE[1]	Output	FPGA configuration mode control signal, M1.
F2	CFG_MODE[2]	Output	FPGA configuration mode control signal, M2.
K1	CFG_CLK	Output	FPGA configuration clock (CCLK). Up to half the SYSCLK rate.
K2	CFG_PROG	Output	FPGA configuration reset signal, PROGRAM. An external 4.7 kΩ pull-up resistor to CFG_VCCO is recommended.
K3	CFG_INIT	Input	FPGA configuration INIT signal monitor. An external 4.7 kΩ pull-up resistor to CFG_VCCO is required.
G1	CFG_BUSY	Input	FPGA SelectMAP configuration BUSY signal monitor.
D4	CFG_DONE	Input	FPGA configuration DONE signal monitor. An external 330Ω pull-up resistor to CFG_VCCO is required.
J3	CFG_DATA[0]	Output	D0 for SelectMAP configuration bus; or DIN for first FPGA on Slave-Serial chain 0.
J2	CFG_DATA[1]	Output	D1 for SelectMAP configuration bus; or DIN for first FPGA on Slave-Serial chain 1.
H4	CFG_DATA[2]	Output	D2 for SelectMAP configuration bus; or DIN for first FPGA on Slave-Serial chain 2.
H3	CFG_DATA[3]	Output	D3 for SelectMAP configuration bus; or DIN for first FPGA on Slave-Serial chain 3.
H2	CFG_DATA[4]	Output	D4 for SelectMAP configuration bus; or DIN for first FPGA on Slave-Serial chain 4.
H1	CFG_DATA[5]	Output	D5 for SelectMAP configuration bus; or DIN for first FPGA on Slave-Serial chain 5.
J4	CFG_DATA[6]	Output	D6 for SelectMAP configuration bus; or DIN for first FPGA on Slave-Serial chain 6.
G4	CFG_DATA[7]	Output	D7 for SelectMAP configuration bus; or DIN for first FPGA on Slave-Serial chain 7.
L1	CFG_WRITE	Output	SelectMAP read/write control signal (RDWR_B). No connect for Slave-Serial configuration.
D3	CFG_CS[0]	Output	SelectMAP chip select 0. Connect to CS on SelectMAP FPGA 0. No connect for Slave-Serial configuration.

Table 5: XCV50E Configuration Pins for Target FPGAs (Continued)

CS144	Pin Name	Type	Description
E1	CFG_CS[1]	Output	SelectMAP chip select 1. Connect to CS on SelectMAP FPGA 1. No connect for Slave-Serial configuration.
D1	CFG_CS[2]	Output	SelectMAP chip select 2. Connect to CS on SelectMAP FPGA 2. No connect for Slave-Serial configuration.
C1	CFG_CS[3]	Output	SelectMAP chip select 3. Connect to CS on SelectMAP FPGA 3. No connect for Slave-Serial configuration.

XCV50E Boundary Scan Pins

Table 6 provides the Boundary Scan pins.

Table 6: XCV50E Boundary Scan Pins

CS144	Pin Name
C3	TCK
B1	TMS
A11	TDI
A12	TDO

XCV50E Power and Ground Pins

Table 7 provides the XCV50E power and ground pins.

Table 7: XCV50E Power and Ground Pins

XCV50E Pin Name	CS144	System ACE Pin Name	Description
VCCINT	A9	VCCint1	1.8V power supply for XCV50E core.
VCCINT	B6	VCCint1	1.8V power supply for XCV50E core.
VCCINT	C5	VCCint1	1.8V power supply for XCV50E core.
VCCINT	G3	VCCint1	1.8V power supply for XCV50E core.
VCCINT	G12	VCCint1	1.8V power supply for XCV50E core.
VCCINT	M5	VCCint1	1.8V power supply for XCV50E core.
VCCINT	M9	VCCint1	1.8V power supply for XCV50E core.
VCCINT	N6	VCCint1	1.8V power supply for XCV50E core.
VCCO (Bank 0)	A2	CTRL_VCCO	1.8V, 2.5V, or 3.3V power supply for control and status pins. Use voltage that is compatible with system control and monitoring logic.
VCCO (Bank 1)	A13	CTRL_VCCO	1.8V, 2.5V, or 3.3V power supply for control and status pins. Use voltage that is compatible with system control and monitoring logic.
VCCO (Bank 1)	D7	CTRL_VCCO	1.8V, 2.5V, or 3.3V power supply for control and status pins. Use voltage that is compatible with system control and monitoring logic.
VCCO (Bank 2)	B12	FLASH_VCCO	3.3V power supply for flash interface pins.
VCCO (Bank 3)	G11	FLASH_VCCO	3.3V power supply for flash interface pins.

Table 7: XCV50E Power and Ground Pins (Continued)

XCV50E Pin Name	CS144	System ACE Pin Name	Description
VCCO (Bank 3)	M13	FLASH_VCCO	3.3V power supply for flash interface pins.
VCCO (Bank 4)	N13	FLASH_VCCO	3.3V power supply for flash interface pins.
VCCO (Bank 5)	N1	FLASH_VCCO	3.3V power supply for flash interface pins.
VCCO (Bank 5)	N7	FLASH_VCCO	3.3V power supply for flash interface pins.
VCCO (Bank 6)	M2	CFG_VCCO	1.8V, 2.5V, or 3.3V power supply for target FPGA configuration interface pins. Use voltage that is compatible with target FPGA configuration pins.
VCCO (Bank 7)	B2	CFG_VCCO	1.8V, 2.5V, or 3.3V power supply for target FPGA configuration interface pins. Use voltage that is compatible with target FPGA configuration pins.
VCCO (Bank 7)	G2	CFG_VCCO	1.8V, 2.5V, or 3.3V power supply for target FPGA configuration interface pins. Use voltage that is compatible with target FPGA configuration pins.
GND	A1	GND	Ground
GND	B9	GND	Ground
GND	B11	GND	Ground
GND	C7	GND	Ground
GND	D5	GND	Ground
GND	E4	GND	Ground
GND	E11	GND	Ground
GND	F1	GND	Ground
GND	G10	GND	Ground
GND	J1	GND	Ground
GND	J12	GND	Ground
GND	L3	GND	Ground
GND	L5	GND	Ground
GND	L7	GND	Ground
GND	L9	GND	Ground
GND	N12	GND	Ground

XCV50E and XC17V01 Configuration Connections

Table 8 provides the XCV50E configuration connections from the XC17V01 device.

Table 8: XCV50E Configuration Connections from the XC17V01¹ Device

XCV50E Pin Name	CS144	XC17V01 Pin Name	VO8	SO20	PC20	External Connection
PROGRAM (FCMRESET)	L12					4.7 k Ω pull-up resistor to 3.3V
M0	M1					GND
M1	L2					GND
M2	N2					GND
DIN/D0	C12	DATA	1	1	1	
CCLK	B13	CLK	2	3	3	
INIT	L13	OE/Reset ²	3	8	8	4.7 k Ω pull-up resistor to 3.3V
DONE (DEV RDY)	M12	/CE	4	10	10	330 Ω pull-up resistor to 3.3V
		GND	5	11	11	GND
		/CEO	6	13	13	No connect
		V _{PP}	7	18	18	3.3V
		V _{CC}	8	20	20	3.3V

Notes:

1. Unlisted XC17V01 pins are no connects, i.e., must not be externally connected.
2. The XC17V01 device must be programmed with an active-low Reset polarity.

Flash Memory Configuration Storage Devices

The System ACE SC supports configuration data storage up to 64 Mb in AMD Flash memories.

XCV50E to AMD Am29LV160D Flash Memory Connections

Table 9 provides the XCV50E to AMD Am29LV160D Flash memory connections.

Table 9: XCV50E to AMD Am29LV160D Flash Memory Connections

XCV50E CS144	Am29LV160D Pin Name	48-Pin TSOP	48-Pin Reverse TSOP	44-Pin SO	48-Ball FBGA	External Connection
L4	A0	25	24	11	E1	
K4	A1	24	25	10	D1	
N3	A2	23	26	9	C1	
M3	A3	22	27	8	A1	
K5	A4	21	28	7	B1	
N4	A5	20	29	6	D2	
K6	A6	19	30	5	C2	
N5	A7	18	31	4	A2	

Table 9: XCV50E to AMD Am29LV160D Flash Memory Connections (Continued)

XCV50E CS144	Am29LV160D Pin Name	48-Pin TSOP	48-Pin Reverse TSOP	44-Pin SO	48-Ball FBGA	External Connection
M6	A8	8	41	42	B5	
M4	A9	7	42	41	A5	
N11	A10	6	43	40	C5	
L10	A11	5	44	39	D5	
L8	A12	4	45	38	B6	
N8	A13	3	46	37	A6	
N9	A14	2	47	36	C6	
K8	A15	1	48	35	D6	
N10	A16	48	1	34	E6	
K9	A17	17	32	3	B2	
L11	A18	16	33	2	C3	
M8	A19	9	40	43	D4	
G13	DQ0	29	20	15	E2	
K13	DQ1	31	18	17	H2	
H13	DQ2	33	16	19	E3	
D11	DQ3	35	14	21	H3	
C13	DQ4	38	11	24	H4	
F13	DQ5	40	9	26	E4	
F10	DQ6	42	7	28	H5	
F11	DQ7	44	5	30	E5	
E12	DQ8	30	19	16	F2	
E13	DQ9	32	17	18	G2	
D13	DQ10	34	15	20	F3	
E10	DQ11	36	13	22	G3	
C12	DQ12	39	10	25	F4	
C11	DQ13	41	8	27	G5	
F12	DQ14	43	6	29	F5	
D12	DQ15/A-1	45	4	31	G6	
	BYTE	47	2	33	F6	3.3V
H11	CE	26	23	12	F1	
H12	OE	28	21	14	G1	
J13	WE	11	38	44	A4	
H10	RESET	12	37	1	B4	External 4.7 kΩ pull-down resistor to 3.3V required.
M11	RY/BY	15	34	N/A	A3	

Table 9: XCV50E to AMD Am29LV160D Flash Memory Connections (Continued)

XCV50E CS144	Am29LV160D Pin Name	48-Pin TSOP	48-Pin Reverse TSOP	44-Pin SO	48-Ball FBGA	External Connection
	V _{CC}	37	12	23	G4	3.3V
	V _{SS}	27, 46	3, 22	13, 32	H1, H6	GND
M10	NC	10	39		D3	
	NC	13	36		C4	
J10	NC	14	35		B3	

XCV50E to AMD Am29LV320D Flash Memory Connections

Table 10 provides the XCV50E device connections to the AMD Am29LV320D Flash memory.

Table 10: XCV50E to AMD Am29LV320D Flash Memory Connections

XCV50E CS144	Am29LV320D Pin Name	48-Pin TSOP	48-Ball FBGA	External Connection
L4	A0	25	E1	
K4	A1	24	D1	
N3	A2	23	C1	
M3	A3	22	A1	
K5	A4	21	B1	
N4	A5	20	D2	
K6	A6	19	C2	
N5	A7	18	A2	
M6	A8	8	B5	
M4	A9	7	A5	
N11	A10	6	C5	
L10	A11	5	D5	
L8	A12	4	B6	
N8	A13	3	A6	
N9	A14	2	C6	
K8	A15	1	D6	
N10	A16	48	E6	
K9	A17	17	B2	
L11	A18	16	C3	
M8	A19	9	D4	
M10	A20	10	D3	
G13	DQ0	29	E2	
K13	DQ1	31	H2	
H13	DQ2	33	E3	

Table 10: XCV50E to AMD Am29LV320D Flash Memory Connections (Continued)

XCV50E CS144	Am29LV320D Pin Name	48-Pin TSOP	48-Ball FBGA	External Connection
D11	DQ3	35	H3	
C13	DQ4	38	H4	
F13	DQ5	40	E4	
F10	DQ6	42	H5	
F11	DQ7	44	E5	
E12	DQ8	30	F2	
E13	DQ9	32	G2	
D13	DQ10	34	F3	
E10	DQ11	36	G3	
C12	DQ12	39	F4	
C11	DQ13	41	G5	
F12	DQ14	43	F5	
D12	DQ15/A-1	45	G6	
	BYTE	47	F6	3.3V
H11	CE	26	F1	
H12	OE	28	G1	
J13	WE	11	A4	
J10	\overline{WP}/ACC	14	B3	
H10	RESET	12	B4	External 4.7 k Ω pull-down resistor to 3.3V required.
M11	RY/\overline{BY}	15	A3	
	V _{CC}	37	G4	3.3V
	V _{SS}	27, 46	H1, H6	GND
	NC	13	C4	Connect to 3.3V for migration to 32 Mb or 64 Mb Flash.

XCV50E to AMD Am29LV641D Flash Memory Connections

Table 11 provides the XCV50E connections to the AMD Am29LV641D Flash memory.

Table 11: XCV50E to AMD Am29LV641D Flash Memory Connections

XCV50E CS144	Am29LV641D Pin Name	48-Pin TSOP	48-Pin Reverse TSOP	External Connection
L4	A0	25	24	
K4	A1	24	25	
N3	A2	23	26	
M3	A3	22	27	
K5	A4	21	28	

Table 11: XCV50E to AMD Am29LV641D Flash Memory Connections (Continued)

XCV50E CS144	Am29LV641D Pin Name	48-Pin TSOP	48-Pin Reverse TSOP	External Connection
N4	A5	20	29	
K6	A6	19	30	
N5	A7	18	31	
M6	A8	8	41	
M4	A9	7	42	
N11	A10	6	43	
L10	A11	5	44	
L8	A12	4	45	
N8	A13	3	46	
N9	A14	2	47	
K8	A15	1	48	
N10	A16	48	1	
K9	A17	17	32	
L11	A18	16	33	
M11	A19	15	34	
M10	A20	10	39	
M8	A21	9	40	
G13	DQ0	29	20	
K13	DQ1	31	18	
H13	DQ2	33	16	
D11	DQ3	35	14	
C13	DQ4	38	11	
F13	DQ5	40	9	
F10	DQ6	42	7	
F11	DQ7	44	5	
E12	DQ8	30	19	
E13	DQ9	32	17	
D13	DQ10	34	15	
E10	DQ11	36	13	
C12	DQ12	39	10	
C11	DQ13	41	8	
F12	DQ14	43	6	
D12	DQ15	45	4	
	V _{IO}	47	2	3.3V
H11	CE	26	23	

Table 11: XCV50E to AMD Am29LV641D Flash Memory Connections (Continued)

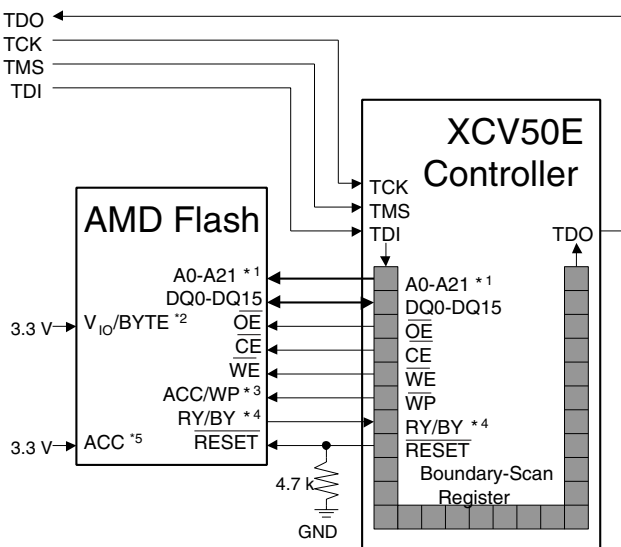
XCV50E CS144	Am29LV641D Pin Name	48-Pin TSOP	48-Pin Reverse TSOP	External Connection
H12	OE	28	21	
J13	WE	11	38	
J10	WP	14	35	
	ACC	13	36	3.3V
H10	RESET	12	37	External 4.7 kΩ pull-down resistor to 3.3V required.
	V _{CC}	37	12	3.3V
	V _{SS}	27, 46	3, 22	GND

System ACE SC and System ACE MPM Differences

IEEE 1149.1 Boundary Scan

The System ACE SC solution pairs an XC17V01 one-time programmable (OTP) PROM with an XCV50E configuration controller. Whereas the System ACE MPM includes an XC18V01 in-system programmable (ISP) PROM in the Boundary Scan chain with the configuration controller, the

System ACE SC controller does not have a companion ISP PROM in the scan chain. Thus, the performance of the System ACE SC Boundary Scan is capable of operating at the faster Boundary Scan frequencies supported in the Virtex-E devices. See Figure 4.



*1 A21 for Am29LV641D only; A20 for Am29LV320D and Am29LV641D only; for A19 on Am29LV641D, see *4.

*2 BYTE on Am29LV160D and Am29LV320D; V_{IO} on Am29LV641D.

*3 No connect on Am29LV160D; ACC/WP on Am29LV320D; /WP on Am29LV641D.

*4 RY/BY on Am29LV160D and Am29LV320D; A19 on Am29LV641D.

*5 ACC for Am29LV641D only.

*6 Boundary-scan register is only conceptually depicted. See the System ACE SC BSDL file for accurate boundary-scan register information.

Figure 4: System ACE SC Boundary Scan Model

Boundary Scan TAP AC Parameters

Table 12 provides the System ACE Boundary Scan TAP AC parameters.

Table 12: System ACE SC Boundary Scan TAP AC Parameters

Symbol	Description	Value	Units
T_{TAPTK}	TMS and TDI setup times before TCK	4	ns, min
T_{TCKTAP}	TMS and TDI hold times after TCK	2	ns, min
T_{TCKTDO}	Delay from TCK to TDO	11	ns, min
F_{TCK}	Maximum TCK frequency	33	MHz, max

System ACE SC MCS Files

Table 13 lists the System ACE SC MCS files for the System ACE SC controller solutions. Use the MCS file to program the XC17V01 PROM that configures the System ACE SC controller.

Table 13: System ACE SC MCS Files

System ACE Controller	Flash Memory	Density	MCS File
XCV50E-6CS144	AMD Am29LV160D	16 Mb	XCCACEM16-CS144-AM.MCS
XCV50E-6CS144	AMD Am29LV320D	32 Mb	XCCACEM32-CS144-AM.MCS
XCV50E-6CS144	AMD Am29LV641D	64 Mb	XCCACEM64-CS144-AM.MCS

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
09/25/01	1.0	Initial Xilinx release.