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Programmable Logic from the INSIDE OUT

Physical Synthesis: The Key to Fast Timing Closure

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Physical synthesis is rapidly becoming a requirement for high-density chip designs. Incons however, between the interconnect timing estimates used during synthesis and the "real" r after the design is physically implemented, are a challenge when trying to get tools to work cooperatively to solve the problem at hand — achieving the fastest timing closure. Two complementary technologies — synthesis and implementation — are required to execute that meet (realistic) performance goals. This week, Justine Chen, a product marketing mar Xilinx Inc., explains physical synthesis technology for programmable logic design solutions

Q: What is physical synthesis? Physical synthesis is an extension of today's familiar synth techniques. In physical synthesis, we augment optimization to "target technology" libraries accurate interconnect delays based on the actual placement of the design. In its most adva physical synthesis enables the simultaneous optimization of HDL code and physical place synthesized logic. This model gives you the ability to most efficiently achieve timing closure implemented design from RTL code. You can create a circuit that meets the realistic perfor goals of the design in just one or two passes. Unfortunately, this "most advanced" model d exist for FPGAs today, but there are some very good approximations that do deliver most of benefits promised by true physical synthesis.

Q: What does Xilinx offer that delivers the benefits of physical synthesis? Circuit delays dominated by net delays, which are influenced by the placement of the cells. The traditional based wireload models for estimating interconnect delay during ASIC synthesis are consid inaccurate for DSM (deep submicron) technologies. In the Xilinx FPGA architectures, the int timing is less variable than in an ASIC. This characteristic makes it possible to create inter models that are not based on fan-out. The models can be used during the synthesis proce estimate with a high degree of predictability the interconnect timing in the placed-and-route Xilinx has partnered with leading FPGA EDA vendors to offer synthesis tools that are aware Xilinx FPGA architectural assets. They use our accurate active interconnect modeling to pro netlists with timing that is within 20% of placed-and-routed designs.

Q: Does Xilinx have any plans to provide a "true" physical synthesis solution? Xilinx is w FPGA EDA vendors to maximize the benefits of physical synthesis technology. We will cont working with these vendors to deliver the ultimate physical synthesis solution.

For more information on physical synthesis and timing closure, see www.xilinx.com/ise