Glossary of Terms

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Term	Definition
Active Interconnect	Xilinx Active Interconnect technology is built on the strength of the fourth-generation segmented routing technology. It provides full buffering at each routing interconnect point. This eliminates the variable routing delay effects of conventional interconnect architectures, where the total routing delay depends on the fan-out. With the conventional interconnect architecture, the routing delay of a particular node may be changed during design iteration, which makes complex designs like the ten million-system gates design impractical. In contrast, Active Interconnect technology allows precise delay calculations that are generally independent of signal fan-out. For complex IP-based designs, Active Interconnect technology allows predictable inter-IP routing delays to facilitate easy integration of multiple complex IP blocks.
ADC	Analog-to-Digital-Converter
AGP	Accelerated Graphics Port. An interface specification from Intel that enables 3-D graphics to display quickly on personal computers. AGP is based on PCI, but is designed especially for the high throughput requirements of 3-D graphics. Rather than using the PCI bus for graphics data, AGP introduces a dedicated point-to-point channel so that the graphics controller can directly access main memory
aliasing	In audio sampling, a distortion-producing reflection caused by the fact that all frequency components higher than half the sampling frequency are reflected in the lower range. Aliasing creates artifacts. It can be avoided by processing the waveform to be sampled with a low-pass filter at half the sample rate before digitizing.
AMPS	1. Advanced Mobile Phone Service (analog). 2. Analog Mobile Phone System. Non-digital cellular mobile phones.
anti-aliasing	In audio applications, the smoothing of steps between discrete samples to reduce the undesirable effects of low bit-rate capture.
artifact	(n.) Evidence of undesirable distortion that appears in digitized audio or video

files as a result of inaccurate information introduced during capture or compression. Artifacts may take the form of new, unwanted data or the degradation of existing content.

ASIC Application Specific Integrated Circuit

ASSP Application Specific Standard Part

ATA Advanced Technology Attachment; a disk drive interface standard for IDE (Integrated Drive Electronics)

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back end (n.) Software that performs the last stage of a process, executing a task that is transparent to the user. The term refers to network applications that run on a server without making the client aware of their operations.

backplane A common bus at the rear of the computer chassis connecting each circuit card slot to the other parts of the system, such as the motherboard on a PCs. It also distributes low-voltage AC and DC, filtered and un-filtered power to each slot. As a rigid circuit board, a backplane can support higher connection speeds and more logic. They are used in large scale network switches and routers.

BIST Built-In Self Test

bitstream The transmission of characters at a fixed rate of speed. No stop and start elements are used, and there are no pauses between bits of data in the stream.

BGA Ball Grid Array. (Sometimes abbreviated BG.) As opposed to a pin grid array (PGA), a ball grid array is a type of microchip connection methodology. Ball grid array chips typically use a group of solder dots, or balls, arranged in concentric rectangles to connect to a circuit board. BGA chips are often used in mobile applications where PGA chips would take up too much space due to the length of the pins used to connect the chips to the circuit board.

boundary scan Boundary scan is a methodology allowing complete controllability and observability of the boundary pins of a JTAG compatible device via software control. This capability enables in-circuit testing without the need of bed-of-nail in-circuit test equipment.

BPSK biphase shift keying. BPSK is a digital frequency modulation technique used for sending data over a coaxial cable network. This type of modulation is less efficient – but also less susceptible to noise – than similar modulation techniques, such as QPSK and 64QAM.

BRAM Buffer Random Access Memory (AT&T)

breadboard To assemble preliminary circuits and parts to prove the feasibility of a device, circuit, or system without regard to the final configuration or packaging of the parts.

bridge A device that forwards traffic between network segments based on (OSI Reference Model) data link layer information. These segments would have a common network layer address. A bridge can connect different kinds of networks (e.g., wireless LAN to Ethernet).

BUFG An architecture-independent global buffer, distributes high fan-out clock signals throughout a PLD device. The Xilinx implementation software converts each BUFG to an appropriate type of global buffer for the target PLD device.

CAM Content Addressable Memory. Also known as "associative memory", CAM is a kind of storage device that includes comparison logic with each bit of storage. A data value is broadcast to all words of storage and compared with the values therein. Words that match are flagged, so that subsequent operations can then work on the flagged words – for example, read them out one at a time or write to certain bit positions in all of them. A CAM can thus operate as a "data parallel" SIMD processor.

CAN bus Controller Area Network Bus?
Campus Area Network

CDMA Code-Division Multiple Access

chip packaging Xilinx internal package designators basically fall into 3 sets:

1. Plastic Leaded Chip Carrier - PC
2. Plastic Quad Flat Pack - PQ, VQ, TQ (varying levels of package height and lead pitch)
3. Ball Grid Array – BG, FG, FT, CS, CP (varying substrate technologies, package height and ball size and pitch

    a. Anything starting with a C is part of the Chip Scale Package family – 0.8mm ball spacing or less
    b. Anything starting with an F is part of the Fine Line BGA family – 1.0mm ball spacing
    c. Anything starting with a B is standard BGA ball spacing – source: Betsy.Thibault@xilinx.com, CoolRunner marketing.

chip scale packaging ball grid array with 0.8 mm or less pitch

CLB Configurable/Complex Logic Block. The array of multi-input and multi-output logic cells to be programmed. In Xilinx terminology, CLB is a configurable logic block. It consists mainly of LUTs and flip flops.

CLK Clock. 1.A circuit in a computer that uses a quartz crystal to generate a series of regular pulses that are sent to the CPU. The clock is the heartbeat of the computer. Switching operations in the computer take place while the clock is sending a pulse. The faster the clock speed, the more instructions per second the computer can execute. 2. A circuit within a computer that keeps track of the date and time, normally powered by a battery so it keeps running when the computer is off.

CLKDLL clock delay-locked loop used to minimize clock skew

CLKFB clock feedback

CMOS Complementary Metal Oxide Semiconductor

codec Short for compressor/decompressor, a codec is any technology for compressing and decompressing data. Codecs can be implemented in software, hardware, or a combination of both. Some popular codecs for computer video include MPEG, Indeo and Cinepak.

In telecommunications, (short for coder/decoder) a device that encodes or decodes a signal. For example, telephone companies use codecs to convert binary signals transmitted on their digital networks to analog signals converted on their analog networks.

The translation of a binary value into a voltage that can be transmitted over a wire.

CompactFlash (CF) A 50-pin connection standard used in some PDAs, digital cameras, hardware MP3 players and other small hardware devices. Initially designed to offer PCMCIA-ATA standard access to flash memory in a smaller form factor than PCMCIA at 43mm x 36mm and thicknesses of 3.3mm (Type I) or 5.5mm (Type II). The standard has been expanded to support other peripherals such as CF modems, CF network cards and other types of I/O devices with the CompactFlash+ standard.

coplanarity Lying or occurring in the same plane. Used of points, lines, or figures.

CPLD Complex Programmable Logic Device

CSMA/CD carrier sense multiple access with collision detection

CSP Chip Scale Packaging. Sometimes abbreviated **CS**.

DAC Digital to Analog Converter. An electronic circuit that converts digital information (for example, from a CD or CD-ROM) into analog information, such as sound and audio signals.

DAQ Data ACquisition

datagram A data packet carrying its own address information so it can be independently routed from its source to the destination computer.

Daughterboard/ daughtercard A printed circuit board that plugs into another circuit board (usually the motherboard). A daughtercard is similar to an expansion board, but it accesses the motherboard components (memory and CPU) directly instead of sending data through the slower expansion bus.

DCM Digital Clock Manager

DDR Double Data Rate (in reference to RAM and registers)

Decimate To discard portions of a signal in order to reduce the amount of information to be encoded or compressed. Lossy compression algorithms ordinarily decimate while subsampling.

DECT Digital Enhanced Cordless Telecommunications: A standard developed by the European Telecommunication Standard Institute from 1988, governing pan-European digital mobile telephony. DECT covers wireless PBXs, telepoint, residential cordless telephones, wireless access to the public switched telephone network, Closed User Groups (CUGs), Local Area Networks, and wireless local loop. The DECT Common Interface radio standard is a multicarrier time division multiple access, time division duplex (MC-TDMA-TDD) radio transmission technique using ten radio frequency channels from 1880 to 1930 MHz, each divided into 24 time slots of 10ms, and twelve full-duplex accesses per carrier, for a total of 120 possible combinations. A DECT base station (an RFP, Radio Fixed Part) can transmit all 12 possible accesses (time slots) simultaneously by using different frequencies or using only one frequency. All signaling information is transmitted from the RFP within a multiframe (16 frames). Voice signals are digitally encoded into a 32 kbit/s signal using Adaptive Differential Pulse Code Modulation.

DES Data Encryption Standard

DFS Digital Frequency Synthesizer

DLL Delay-Locked Loop (aka digital delay-locked loops)
Dynamic Link Library

DMA Direct Memory Access/Addressing. DMA is a method of transferring data from one memory area to another without having to go through the central processing unit. Computers with DMA channels can transfer data to and from devices much more quickly than those in which the data path goes through the computer's main processor.

DPS Digital Phase Shifter

DRAM Dynamic Random Access Memory (pronounced DEE-ram)

DSP 1.Digital Signal Processing. Using computers to process signals such as

	sound, video, and other analog signals which have been converted to digital form. Some uses of DSP are to decode modulated signals from modems, to process sound, video, and images in various ways, and to understand data from sonar, radar, and seismological readings. 2.Digital Signal Processor. A specialized CPU used for digital signal processing. Some uses of digital signal processors are with modems and sound boards.
DSS	digital spread spectrum (cordless phone technology)
DVR	Digital Video Recorder/Recording. Also, Driver

EDA	Electronic Design Automation. <applicationSoftware tools for the development of integrated circuits and systems.
EDIF	Electronic Design Interchange Format

fabric	The arrangement and physical relationship of components or constituent elements of something.
FAE	field application engineers
Fan-in	A board or other device that gathers signals from a variety of devices and consolidates them for processing (as with an MADC).
Fan-out	A board or other device which receives a signal, replicates it, and sends it out to a number of devices.
Fan-in and Fan-out	A fan-in is a module that performs the function of linearly adding either analog or logic signals. A fan-in is often used to perform high-order majority logic decision. (e.g., any 6 out of 32) by attenuating each input and discriminating on the summed output. (Many inputs, few outputs.) A fan-out is a module used to distribute a fast signal to several 50W loads with no loss in signal amplitude. (Few inputs, many outputs.)
FEC	Forward Error Correction <algorithm>. A class of methods for controling errors in a one-way communication system. FEC sends extra information along with the data, which can be used by the receiver to check and correct the data.
FEPROM	Flash Erasable Programmable Read-Only Memory. See flash memory.
FFT	Fast Fourier Transform. An algorithm for computing the Fourier transform of a set of discrete data values. Given a finite set of data points, for example a periodic sampling taken from a real-world signal, the FFT expresses the data in terms of its component frequencies. It also solves the essentially identical inverse problem of reconstructing a signal from the frequency data.
FIFO	first-in first-out (as opposed to LIFO – last-in first-out) A data structure or hardware buffer where items come out in the same order they came in.
FIR	Finite Impulse Response (filter)
FireWire	The former name for High Performance Serial Bus. A serial bus developed by Apple Computer and Texas Instruments (IEEE 1394). The High Performance Serial Bus can connect up to 63 devices in a tree-like daisy chain configuration, and transmit data at up to 400 megabits per second.It supports plug-and-play and peer-to-peer communication between
flash memory	non-volatile storage device similar to EEPROM, but where erasing can only be done in blocks or the entire chip. *Not capitalized*.
Flash	Macromedia software for creating vector graphics animation
flip chip	A surface mount chip technology where the chip is packaged in place on the

board and then underfilled with an epoxy. A common technique for attachment is to place solder balls on the chip, "flip" the chip over onto the board and melt the solder.

flip-flop A digital logic circuit that can be switched back and forth between two states.

FOLS Fiber Optic LAN Section (Telecommunications Industry Association)

footprint In BGAs, this is the mechanical location of balls on a BGA package.

FPO For Position Only: In printing, a layout term to indicate a temporary graphic has been inserted as a placeholder until the final graphic becomes available. Using FPO images allows an article to be typeset before graphics become available.

FSK Frequency Shift Keying. The use of frequency modulation to transmit digital data, i.e. two different carrier frequencies are used to represent zero and one. FSK was originally used to transmit teleprinter messages by radio (RTTY) but can be used for most other types of radio and land-line digital telegraphy. More than two frequencies can be used to increase transmission rates.

FSM Finite State Machine. For detailed explanation, see the definition in the Free On-line Dictionary of Computing

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gate (n.) In electronic circuitry, a pathway that may be open or closed, depending on the source of the input, the strength of a signal, or the conductivity of chemicals used in semiconductors. Logic gates are programmed to correspond to related"if-then" statements. The state of an open or closed gate is analogous to the binary state of a 0 or a 1. The application of this analogy allows computing machinery with millions of gates to respond conditionally and to perform logical functions.

glue Generic term for any interface logic or protocol that connects two component blocks. Hardware designers call anything used to connect large VLSIs or circuit blocks "glue logic."

GPRS General Packet Radio Service. A GSM data transmission technique that does not set up a continuous channel from a portable terminal for the transmission and reception of data, but transmits and receives data in packets. It makes very efficient use of available radio spectrum.

GSM Global System for Mobile Communications. A standard for digital cellular communications (in the process of being) adopted by over 60 countries. The GSM standard is currently used in the 900 MHz and 1800 MHz bands. (GSM, originally"Groupe de travail Spéciale pour les services Mobiles".)

GTL Gunning Transceiver Logic is a standard for electrical signals in CMOS circuits that is used to provide high data transfer speeds with small voltage swings.

H.323 An ITU-T standard for transferring multimedia videoconferencing data over packet-switched networks, such as TCP/IP.

HDL Hardware Description Language. A kind of language used for the conceptual design of integrated circuits. Examples are VHDL and Verilog.

hex aka **hexadecimal** The base 16 numbering system, sometimes used as a short way of representing binary numbers. The digits 0-9 are used, plus the letters A-F which stand for numbers 10 to 15. The farthest-right digit is the ones place; the digit next to the left is the 16s place; the next place to the left is 16^2 = 256, etc. Each place is 16 times the place immediately to the right of it.

HLL high-level language – Any programming language in which a single statement may be translated into numerous assembly language or machine code instructions. High-level languages are designed to be machine-independent, in contrast to an assembly language. C++, BASIC, Pascal, and FORTRAN are examples of high-level languages.

HSTL High Speed Transistor Logic

HUD Heads-Up Display

IBUF input buffer. An IBUF isolates the internal circuit from the signals coming into a chip.

ICON Integrated CONtrol (in re: ICON core)

IEEE 802.11 In wireless LAN (WLAN) technology, 802.11 refers to a family of specifications developed by a working group of the Institute of Electrical and Electronics Engineers (IEEE). There are three specifications in the family: 802.11, 802.11a, and 802.11b.

All three of the specifications use carrier sense multiple access with collision detection (CSMA/CD) as the path sharing protocol. The 802.11 and 802.11b specifications apply to wireless Ethernet LANs, and operate at frequencies in the 2.4-GHz region of the radio spectrum. The modulation used in 802.11 has historically been phase-shift keying (PSK). The modulation method selected for 802.11b is known as CCK (complementary code keying), which allows higher data speeds and is less susceptible to multipath-propagation interference.

The 802.11a specification applies to wireless ATM systems and operates at radio frequencies between 5 GHz and 6 GHz.

IEEE 1394 FireWire™ A high performance serial bus for plug-and-play and peer-to-peer networks.

ILA Integrated Logic Analysis (as in ChipScope ILA debugging tool)

impedance The combined effect of capacitance, inductance, and resistance on a signal. According to Ohm’s law, voltage is the product of current and resistance at a given frequency.
Impedance is a measure of resistance to electrical current flow when a voltage is moved across it. Impedance is measured in ohms and is the ratio of voltage to the flow of current allowed.

instantiate / instantiation In programming, to produce a more defined version of an object by replacing variables with values (or other variables). As used in logic programming, this means to bind a logic variable (type variable) to some value (type).

IOB Input Output Buffer or Input/Output Block in an FPGA

IP Internet Protocol (as in TCP/IP)
Intellectual Property (as in IP core)

IrDA Infrared Data Association, a group of device manufacturers that developed a standard for transmitting data via infrared light waves.

ISE Integrated Synthesis Environment

ISP In-System Programming
Internet Service Provider

JTAG Joint Test Action Group <architecture, body, electronics, integrated circuit, standards, testing> (JTAG, or"IEEE Standard 1149.1") A standard specifying how to control and monitor the pins of compliant devices on a printed circuit board.

LAQ lame ass quote. Overused, meaningless jargon and buzz phrases used by high-tech executives and media types.

LFSR Linear Feedback Shift Register

LUT Look-Up Table. An array or matrix of values that contains data that is searched. An alternative implementation of a CLB; the multiple inputs generate the complex outputs.

LVCMOS Low Voltage Complementary Metal Oxide Semiconductor

LVDS Low Voltage Differential Signaling

LVTTL Low Voltage Transistor - Transistor Logic

MAC

1. Multiply-and-Accumulate. Used in Xilinx DSP applications to denote MACs per second – e.g.: one trillion multiply-and-accumulate operations per second (1 Tera MACs/sec).
2. Media Access Control. The lower sublayer of the OSI data link layer. The interface between a node's Logical Link Control and the network's physical layer. The MAC differs for various physical media.

macrocell A macrocell on most modern CPLDs contains a sum-of-products combinatorial logic function and an optional flip-flop. The combinatorial logic function typically supports four to sixteen product terms with wide fan in. Thus, a macrocell may have many inputs, but the logic function complexity is limited. On the other hand, most FPGA logic blocks have unlimited complexity, but the logic function only has four inputs.

Mb megabit

MB megabyte

microstrip A thin, striplike transmission line used for transmitting microwave frequencies; typically mounted on a flat dielectric substrate that is mounted on a ground plane.

microcontroller A highly integrated chip that contains all the components comprising a controller. Typically, this includes a CPU, RAM, some form of ROM, I/O ports, and timers. Unlike a general-purpose computer, which also includes all of these components, a microcontroller is designed for a very specific task – to control a particular system. As a result, the parts can be simplified and reduced, which cuts down on production costs. Microcontrollers are sometimes called embedded microcontrollers, which just means that they are part of an embedded system – that is, one part of a larger device or system.

MII Media Independent Interface – something to do with the OSI model?

MIPS Million Instructions Per Second … or Meaningless Indicator of Performance

MMT MultiMedia Terminal

modulo arithmetic (Or"clock arithmetic") A kind of integer arithmetic that reduces all numbers to one of a fixed set [0...N-1] (this would be"modulo N arithmetic") by effectively repeatedly adding or subtracting N until the result is within this range. Ordinary"clock arithmetic" is like modulo arithmetic except that the range is [1...12] whereas modulo 12 would be [0..11].

MOSFET A Metal Oxide Semiconductor Field Effect Transistor in which the conducting channel is insulated from the gate terminal by a layer of oxide. Therefore, it does not conduct even if a reverse voltage is applied to the gate.

MSB Most Significant Bit. In a binary number, this is the bit that is the farthest to the left, and has the greatest weight.

MSPS Mega Samples Per Second?

MTU Maximum Transmission Unit. The largest unit of data that can be transmitted on any particular physical medium.

mu A Greek letter used as a prefix, meaning micro- (millionth). When using only

ASCII characters, it is represented by lowercase u, which looks the most like the Greek letter "μ". You can insert a real "μ" by typing "m" in the Symbol font.

multiplexer (MUX). A hardware device that enables two or more signals (analog or digital) to be transmitted over the same circuit by temporarily combining them into a single signal. On the receiving end, the signals are divided again by a demultiplexer.

1. **FDM** - Frequency Division Multiplexing: each signal is assigned a different frequency.
2. **TDM** - Time Division Multiplexing: each signal is assigned a fixed time slot in a fixed rotation
3. **STDM** - Statistical Time Division Multiplexing: time slots are assigned to signals dynamically to make better use of bandwidth
4. **WDM** - Wavelength Division Multiplexing: each signal is assigned a particular wavelength; used on optical fiber

MUX same as a mutiplexer

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netlist A list of names of symbols or parts and their connection points, which are logically connected in each net of a circuit. A file listing parameters extracted from a circuit schematic.

nonvolatile not hyphenated

OC Optical Carrier. The transmission speeds defined in the SONET specification. OC defines transmission by optical devices, and STS is the electrical equivalent.

OC-192 Optical Carrier 192 (10 Gbits/Sec)

ohm A unit of electrical resistance; the resistance of a conductor in which a potential difference of one volt produces a current of one ampere.

onboard adjective or adverb – no hyphen

OSI-RM Open Systems Interconnect Reference Model, a model of network architecture and a suite of protocols (a protocol stack) to implement it, developed by ISO in 1978 as a framework for international standards in heterogeneous computer network architecture. The OSI architecture is a series of non-proprietary protocols and specifications that are split into seven layers, from lowest to highest: 1 physical layer, 2 data link layer, 3 network layer, 4 transport layer, 5 session layer, 6 presentation layer, 7 application layer. Each layer uses the layer immediately below it and provides a service to the layer above. In some implementations a layer may itself be composed of sub-layers.

PAR place-and-route

PCI Peripheral Component Interconnect. A personal computer local bus designed by Intel, which runs at 33 MHz and supports Plug and Play. It provides a high-speed connection with peripherals and allows connection of seven peripheral devices. It is mostly used with Pentium computers but is processor independent and therefore able to work with other processors. It plugs into a PCI slot on the motherboard and can be used along with an ISA or EISA bus.

PCMCIA Personal Computer Memory Card International Association; pronounced as separate letters. A standard for small, credit card-sized devices, called PC Cards. Originally designed for adding memory to portable computers, the PCMCIA standard has been expanded several times and is now suitable for many types of devices. There are in fact three types of PCMCIA cards. All three have the same rectangular size (85.6 by 54 millimeters), but different widths. Alternative meaning: People Can't Memorize Computer Industry Acronyms.

PCS Personal Communication Services. Wireless communications services that use the 1900 MHz (1.9 GHz) band rather than the 800 MHz used for cellular, and that use digital technology for transmission and reception.

PGA pin grid array. See BGA. PGA is a style of integrated circuit socket or pinout with pins laid out on a square or rectangular grid with a separation of 0.1 inch in each direction. The pins near the center of the array are often missing.

pinout A diagram that indicates how wires are terminated to pins in a connector. A list that assigns device functions to specific BGA balls or pins.

pitch Pitch refers to center-to-center distance between adjacent solder balls in chip scale packaging.

pipeline processing A method of parallel data processing in which a task is divided into segments. The output of one stage is input to the next stage. This speeds up processing by allowing several segments of the tasks to run simultaneously.

Platform FPGA A Xilinx initiative, Platform FPGA is a flexible solution that integrates a wide variety of hard and soft intellectual property (IP) cores on a single device whose hardware and firmware can be upgraded at any time. A single Platform FPGA can be targeted at multiple applications. Involves Virtex™-II devices, IP Immersion, and Active Interconnect.

PLCC Plastic Leadless Chip Carrier. A less expensive version of the leadless chip carrier, which is a square chip housing with flat contacts, instead of pin connectors, on each side. Sometimes abbreviated **PC**

PLL Phased-Locked Loops

PQFP Plastic Quad Flat Pack chip carrier. Sometimes abbreviated **PQ**.

PVR Personal Video Recorder

QFP Quad Flat Pack, a fine-pitch SMT (Surface Mount Technology) package that is rectangular or square with gull-wing shaped leads on all four sides.

QoR Quality of Results

QPSK quadrature phase shift keying. QPSK is a digital frequency modulation technique used for sending data over coaxial cable networks. Since it's both easy to implement and fairly resistant to noise, QPSK is used primarily for sending data from the cable subscriber upstream to the Internet. Compare to BPSK.

quantization The process of converting, or digitizing, the almost infinitely variable amplitude of an analog waveform to one of a finite series of discrete levels. In video compression, a process that attempts to determine what information can be discarded safely without a significant loss in visual fidelity. Quantization uses DCT coefficients and provides many-to-one mapping. The quantization process is inherently lossy because of the many-to-one mapping process.

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register

1. One of a small number of high-speed memory locations in a computer's CPU. Registers differ from ordinary random access memory in several respects:

   There are only a small number of registers (the "register set"), typically 32 in a modern processor though some, e.g. SPARC, have as many as 144. A register may be directly addressed with a few bits. In contrast, there are usually millions of words of main memory (RAM), requiring at least twenty bits to specify a memory location. Main memory locations are often specified indirectly, using an indirect

addressing mode where the actual memory address is held in a register.

Registers are fast; typically, two registers can be read and a third written -- all in a single cycle. Memory is slower; a single access can require several cycles.

The limited size and high speed of the register set makes it one of the critical resources in most computer architectures. Register allocation, typically one phase of the back-end, controls the use of registers by a compiled program.

2. An addressable location in a memory-mapped peripheral device. E.g. the transmit data register in a UART.

RS-232 Recommended Standard 232. This is the de facto standard for communication through PC serial ports. It can refer to cables and ports that support the RS-232 standard.

RTL Register Transfer Level/Language (software) A kind of hardware description language (HDL) used in describing the registers of a computer or digital electronic system, and the way in which data is transferred between them. An intermediate code for a machine with an infinite number of registers. Register Transfer Level (VHDL)

Resistor Transistor Logic (hardware)

Right-to-Left

sample rate (n.) The frequency at which bits of data are recorded in digitizing a sound. Normally, sound is sampled at 44.1 kHz. To reduce the amount of space required to store audio data, rates of 22.050 kHz and 11.025 kHz are used. These rates yield lower quality and are not advisable for high-fidelity music. When a sample encoded at a given bit rate is converted to a higher or a lower rate, some noise is introduced, but this is not nearly as serious as the artifacts generated in bit-rate conversion from 16-bit to 8-bit audio.

Sampling (n.) Measuring an analog signal periodically or obtaining the values of an analog function by regularly measuring the function. Sampling is a step in the process of converting an analog signal into a digital one. The other steps are quantizing and encoding. Sampling errors can cause aliasing effects and artifacts.

SDH Synchronous Digital Hierarchy. SDH is the international standard for transmitting digital information over optical networks. It refers to the ITU term for the ANSI standard, SONET.

SDRAM [S-D-RAM] Synchronous Dynamic Random Access Memory

SIMD Single Instruction/Multiple Data ("data parallel"). A parallel processor where many processing elements (functional units) perform the same operations on different data. Often a central controller broadcasts the instruction stream to all the processing elements.

SMBus System Management Bus

SMT Surface Mount Technology for PCBs

SNR signal-to-noise ratio. A high signal-to-noise ratio is a good thing.

SoC System on Chip

SOIC Small-Outline Integrated Circuit

SONET Synchronous Optical Network. SONET allows telecommunications products from different vendors to communicate over high-speed fiber optic networks.

SPROM Serial configuration PROM

SRAM Static Random Access Memory, a type of memory that is faster and more reliable than the more common DRAM (dynamic RAM). The term static is derived from the fact that it doesn't need to be refreshed like dynamic RAM, but it loses its memory if it's powered off.

SSTL Solid State Track Link

System ACE™ System Advanced Configuration Environment. System ACE consists of two components: ACE Flash™ memory module and ACE Controller™ chip. System ACE is a space-efficient, pre-engineered, high-density configuration bitstream manager for multi-FPGA systems. The system can be upgraded or debugging by either exchanging the ACE Flash module or reprogramming the module in-system.

TCP Transmission Control Protocol. This is one of the main protocols in TCP/IP networks. IP protocol deals only with packets. TCP allows two hosts to establish a connection and exchange streams of data. TCP guarantees that delivery of data and packets will be delivered in the same order in which they were sent.

TDMA Time Division Multiple Access, a technology for delivering digital wireless service using time division multiplexing. TDMA works by dividing a radio frequency into discrete time slots and then allocating slots to multiple calls. This allows a single frequency to support multiple, simultaneous data channels. TDMA is used by the GSM digital cellular system.

ternary an operator taking three arguments: "0", "1", and "don't care".

tPD pin-to-pin delay??? (measured in nanoseconds) (re: CoolRunner XPLA3)

TQFP Thin Quad Flat Pack, chip carrier; sometimes abbreviated **TQ**

trace A line or"wire" of conductive material – such as copper, silver, or gold – on the surface of or sandwiched inside a PCB, printed circuit board. These traces are often called individually a run. Traces carry an electronic signal or other forms of electron flow from one point to another. Traces that are on the surface of a board are covered with a non-conductive coating, except at contact or solder points, to keep unintentional contact from being made with other conductive surfaces.

TSOP Thin Small Outline Package (chip carrier)

UART Universal Asynchronous Receiver Transmitter. This is a chip that standardized serial communications. Its function is to change a byte into a standard sequence of electrical impulses.

UCF User Constraints File

UDP User Datagram Protocol. Connectionless protocol that, like TCP, runs on top of IP networks. Unlike TCP/IP, UDP/IP provides very few error recovery services, offering instead a direct way to send and receive datagrams over an IP network. It's used primarily for broadcasting messages over a network.

USB Universal Serial Bus. An external peripheral interface standard for Plug-and-Play communication between a computer and external peripherals over a cable using bi-directional serial transmission at speeds of 12 Mbps.

UTOPIA **U**niversal **T**est and **O**peration **P**HY-**I**nterface for **A**TM

Verilog A Hardware Description Language for electronic design and gate-level

simulation by Cadence Design Systems.

VQFP Very small Quad Flat Package

VHDL Very High Speed Integrated Circuit (VHSIC) Hardware Description Language

VHSIC Very High Speed Integrated Circuit

via Feed-through. A plated through-hole in a printed circuit board used to route a trace vertically in the board, that is, from one layer to another.

VIA Virtual Interface Architecture [Intel]

VLSI Very large-scale integration, the process of placing thousands (or hundreds of thousands) of electronic components on a single chip. Nearly all modern chips employ VLSI architectures, or ULSI (ultra large scale integration).

VME

1. **Versa Module Eurocard bus.** A 32-bit bus developed by Motorola, Signetics, Mostek, and Thompson CSF. It is widely used in industrial, commercial, and military applications with more than 300 manufacturers of VMEbus products worldwide. It is defined by the IEEE standard 1014-1987. VME64 is an expanded version that provides 64-bit data transfer and addressing.
2. **Virtual Machine Environment.** International Computers Limited plc. A multinational UK hardware and software manufacturer specialising in systems integration in selected markets, supported by its service and technology businesses. A mainframe operating system.

vocoder Hardware or software which implements a compression algorithm particular to voice.

VoIP Voice over Internet Protocol

WAP Wireless Application Protocol. An open international standard for applications that use wireless communication, e.g. Internet access from a mobile phone.

.wmf Windows Metafile Format. This is a graphics file format used to exchange graphics information between Microsoft Windows applications.

XCITE Xilinx Controlled Impedance TEchnology: built-in digitally controlled impedance (DCI) matching on all single-ended I/Os for signal integrity. XCITE eliminates the need for external termination resistors by incorporating adaptive series and parallel termination resistors on the FPGA itself. The on-chip resistor values are completely user definable via an external pair of reference resistors.

XPLA eXtended Programmable Logic Array. As in CoolRunner XPLA3.

ZBT Zero Bus Turnaround (ZBT) is a synchronous SRAM architecture optimized for networking and telecommunications applications.