

## Package Information

### Inches vs. Millimeters

The JEDEC standards for PLCC, CQFP, and PGA packages define package dimensions in inches. The lead spacing is specified as 25, 50, or 100 mils (0.025", 0.050" or 0.100").

The JEDEC standards for PQFP, HQFP, TQFP, and VQFP packages define package dimensions in millimeters. These packages have a lead spacing of 0.5 mm, 0.65 mm, or 0.8 mm.

Because of the potential for measurement discrepancies, this Data Book provides measurements in the controlling standard only, either inches or millimeters. (See [Table 1](#) for package dimensions.)

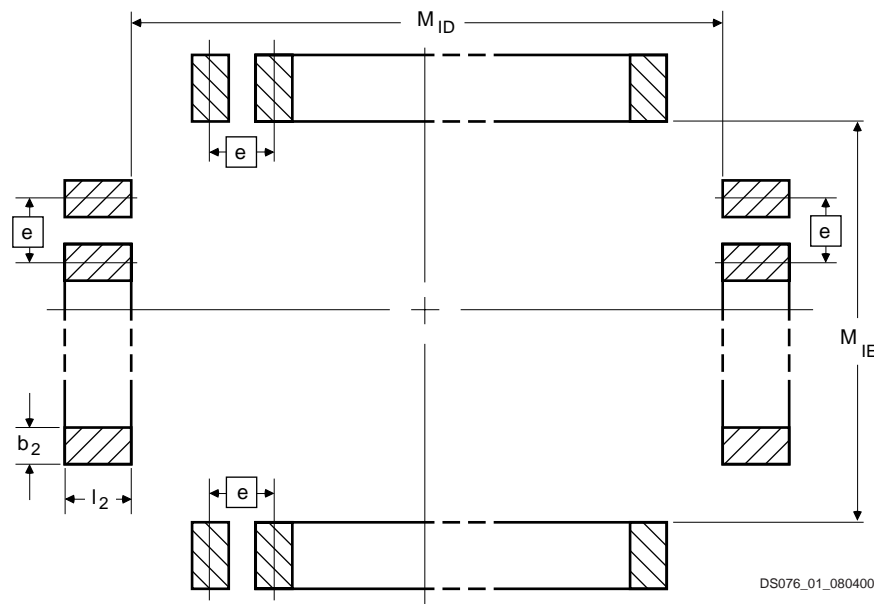


Figure 1: EIA Standard Board Layout of Soldered Pads for QFP Devices

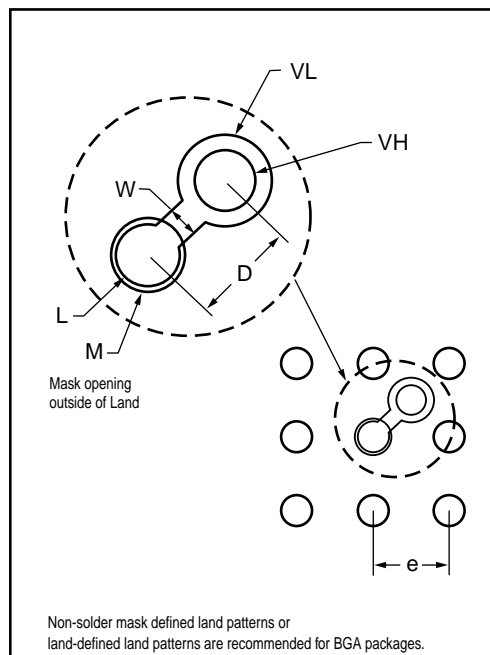
Table 1: Dimensions for Xilinx Quad Flat Packs<sup>(1)</sup>

Dim.	VQ44	VQ64	PQ100	HQ160	HQ208	VQ100	TQ144	TQ176	HQ240	HQ304
$M_{ID}$	9.80	9.80	20.40	28.40	28.20	13.80	19.80	23.80	32.20	40.20
$M_{IE}$	9.80	9.80	14.40	28.40	28.20	13.80	19.80	23.80	32.20	40.20
e	0.80	0.50	0.65	0.65	0.50	0.50	0.50	0.50	0.50	0.50
$b_2$	0.4-0.6	0.3-0.4	0.3-0.5	0.3-0.5	0.3-0.4	0.3-0.4	0.3-0.4	0.3-0.4	0.3-0.4	0.3-0.4
$l_2$	1.60	1.60	1.80 <sup>(2)</sup>	1.80	1.60	1.60	1.60	1.60	1.60	1.60

**Notes:**

1. Dimensions in millimeters..
2. For 3.2 mm footprint per MS022, JEDEC Publication 95.

## Suggested Board Layout of Soldered Pads for BGA Packages



DS076\_02\_050301

Figure 2: Suggested Board Layout of Soldered Pads for BGA Packages

Table 2: Recommended PCB Design Rules

	FG256	FG456	FG676	FG680	FG860	FG900	FG1156	FF896	FF1152	FF1517
Component Land Pad Diameter (SMD) 4	0.45	0.45	0.45	0.50	0.50	0.45	0.45	0.58	0.58	0.58
Solder Land (L) Diameter	0.40	0.40	0.40	0.40	0.40	0.40	0.40	0.50	0.50	0.50
Opening in Solder Mask (M) Diameter	0.50	0.50	0.50	0.50	0.50	0.50	0.50	0.60	0.60	0.60
Solder (Ball) Land Pitch (e)	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
Line Width Between Via and Land (w)	0.13	0.13	0.13	0.13	0.13	0.13	0.13	0.13	0.13	0.13
Distance Between Via and Land (D)	0.70	0.70	0.70	0.70	0.70	0.70	0.70	0.70	0.70	0.70
Via Land (VL) Diameter	0.61	0.61	0.61	0.61	0.61	0.61	0.61	0.61	0.61	0.61
Through Hole (VH), Diameter	0.300	0.300	0.300	0.300	0.300	0.300	0.300	0.300	0.300	0.300
Pad Array	Full	Full	Full	Full	Full	Full	Full	Full	Full	Full
Matrix or External Row	16 x 16	22 x 22	26 x 26	39 x 39	42 x 42	30 x 30	34 x 34	30 x 30	34 x 34	39 x 39
Periphery Rows	-	73	-	5	6	-	-	-	-	-

Table 2: Recommended PCB Design Rules (Continued)

	BG225	BG256	BG352	BG432	BG560	BG575	BG728	BF957	CS144	CP56
Component Land Pad Diameter(SMD)4	0.63	0.63	0.63	0.63	0.63	0.61	0.61	0.61	0.35	0.30
Solder Land (L) Diameter(NSMD)	0.58	0.58	0.58	0.58	0.58	0.56	0.56	0.56	0.33	0.27
Opening in Solder Mask (M) Diameter	0.68	0.68	0.68	0.68	0.68	0.66	0.66	0.66	0.44	0.35
Solder (Ball) Land Pitch (e)	1.50	1.27	1.27	1.27	1.27	1.27	1.27	1.27	0.80	0.50
Line Width Between Via and Land (w)	0.300	0.203	0.203	0.203	0.203	0.203	0.203	0.203	0.13	0.13
Distance Between Via and Land (D)	1.06	0.90	0.90	0.90	0.90	0.90	0.90	0.90	0.56	-
Via Land (VL) Diameter	0.65	0.65	0.65	0.65	0.65	0.65	0.65	0.65	0.51	0.51
Through Hole (VH), Diameter	0.356	0.356	0.356	0.356	0.356	0.356	0.356	0.356	0.250	0.250
Pad Array	Full	-	-	-	-	Full	Full	Full	-	-
Matrix or External Row	15 x 15	20 x 20	26 x 26	31 x 31	33 x 33	24 x 24	27 x 27	31 x 31	13 x 13	10 x 10
Periphery Rows	-	4	4	4	5				4	1

## Cavity Up or Cavity Down

Most Xilinx devices attach the die against the inside bottom of the package (the side that does not carry the Xilinx logo). This is called cavity-up, and has been the standard IC assembly method for over 25 years. This method does not provide the best thermal characteristics. Pin Grid Arrays (greater than 130 pins) and Ceramic Quad Flat Packs are assembled "Cavity Down", with the die attached to the inside top of the package, for optimal heat transfer to the ambient air.

For most packages this information does not affect how the package is used because the user has no choice in how the package is mounted on a board. For Ceramic Quad Flat Pack (CQFP) packages however, the leads can be formed to either side. Therefore, for best heat transfer to the surrounding air, CQFP packages should be mounted with the logo up, facing away from the PC board.

## Clockwise or Counterclockwise

The orientation of the die in the package and the orientation of the package on the PC board affect the PC board layout. PLCC and PQFP packages specify pins in a counterclockwise direction, when viewed from the top of the package (the surface with the Xilinx logo). PLCCs have pin 1 in the center of the beveled edge while all other packages have pin 1 in one corner, with one exception: The 100-pin and 165-pin CQFPs (CB100 and CB164) for the XC3000 devices have pin 1 in the center of one edge.

CQFP packages specify pins in a clockwise direction, when viewed from the top of the package. The user can make the pins run counterclockwise by forming the leads such that the logo mounts against the PC board. However, heat flow

to the surrounding air is impaired if the logo is mounted down.

## Thermal Management

Modern high-speed logic devices consume an appreciable amount of electrical energy. This energy invariably turns into heat. Higher device integration drives technologies to produce smaller device geometry and interconnections. With smaller chip sizes and higher circuit densities, heat generation on a fast switching CMOS circuit can be very significant. The heat removal needs for these modern devices must be addressed.

Managing heat generation in a modern CMOS logic device is an industry-wide pursuit. However, unlike the power needs of a typical Application Specific Integrated Circuit (ASIC) gate array, the power requirements for FPGAs are not determined as the device leaves the factory. Designs vary in power needs.

There is no way of anticipating the power needs of an FPGA device short of depending on compiled data from previous designs. For each device type, primary packages are chosen to handle "typical" designs and gate utilization requirements. For the most part the choice of a package as the primary heat removal casing works well.

Occasionally designers exercise an FPGA device, particularly the high gate count variety, beyond "typical" designs. The use of the primary package without enhancement may not adequately address the device's heat removal needs. Heat removal management through external means or an alternative enhanced package should be considered.

Removing heat ensures the functional and maximum design temperature limits are maintained. The device may

go outside the temperature limits if heat build up becomes excessive. As a consequence, the device may fail to meet electrical performance specifications. It is also necessary to satisfy reliability objectives by operating at a lower temperature. Failure mechanisms and the failure rate of devices depend on device operating temperature. Control of the package and the device temperature ensures product reliability.

## Package Thermal Characterization Methods and Conditions

### Method and Calibration

Xilinx uses the indirect electrical method for package thermal resistance characterization. The forward-voltage drop of an isolated diode residing on a special test die is calibrated at constant forcing current of 0.520 mA with respect to temperature over a correlation temperature range of 22°C to 125°C (degree Celsius). The calibrated device is then mounted in an appropriate environment (still air, forced convection, circulating FC-40, etc.) Depending on the package, between 0.5 to 4 watts of power ( $P_D$ ) is applied. Power ( $P_D$ ) is applied to the device through diffused resistors on the same thermal die. The resulting rise in junction temperature is monitored with the forward-voltage drop of the precalibrated diode. Typically, three identical samples are tested at each data point. The reproducibility error in the setup is within 6%.

### Definition of Terms

**Junction Temperature ( $T_J$ )** — The maximum temperature on the die, expressed in °C (degree Celsius).

**Ambient Temperature ( $T_A$ )** — Expressed in °C.

**The temperature of the package body ( $T_C$ )** taken at a defined location on the body. This is taken at the primary heat flow path on the package and represents the hottest part on the package — expressed in °C.

**The isothermal fluid temperature ( $T_I$ )** when junction to case temperature is taken — expressed in °C.

**The total device power dissipation ( $P_D$ )** — expressed in watts.

## Junction-to-Reference General Setup

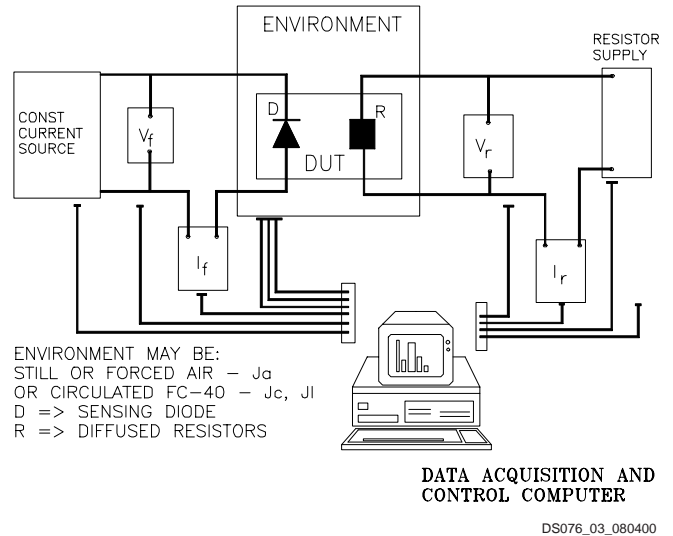


Figure 3: Junction-to-Reference General Setup

## Junction-to-Case Measurement — $\Theta_{JC}$

$\Theta_{JC}$  is measured in a 3M Flourinert (FC-40) isothermal circulating fluid stabilized at 25°C. The Device Under Test (DUT) is completely immersed in the fluid and initial stable conditions are recorded.  $P_D$  is then applied. Case temperature ( $T_C$ ) is measured at the primary heat-flow path of the particular package. Junction temperature ( $T_J$ ) is calculated from the diode forward-voltage drop from the initial stable condition before power was applied.

$$\Theta_{JC} = (T_J - T_C)/P_D$$

The junction-to-isothermal-fluid measurement ( $\Theta_{JI}$ ) is also calculated from the same data.

$$\Theta_{JL} = (T_J - T_I)/P_D$$

The latter data is considered as the ideal  $\Theta_{JA}$  data for the package that can be obtained with the most efficient heat removal scheme. Other schemes such as airflow, heatsinks, use of copper clad board, or some combination of all these will tend towards this ideal figure. Since this is not a widely used parameter in the industry, and it is not very realistic for normal application of Xilinx packages, the  $\Theta_{JI}$  data is not published. The thermal lab keeps such data for package comparisons.

## Junction-to-Ambient Measurement — $\Theta_{JA}$

$\Theta_{JA}$  is measured on FR4 based PC boards measuring 4.5" x 6.0" x .0625" (114.3mm x 152.4mm x 1.6mm) with edge connectors. There are two main board types.

Type I, 2L/0P board, is single layer with two signal planes (one on each surface) and no internal Power/GND planes. The trace density on this board is less than 10% per side. Type II, the 4L/2P board, has two internal copper planes

(one power, one ground) and two signal trace layers on both surfaces.

Data may be taken with the package mounted in a socket or with the package mounted directly on the board. Socket measurements typically use the 2L/0P boards. SMT devices may use either board. Published data always reflects the board and mount conditions used.

Data is taken at the prevailing temperature and pressure conditions (22°C to 25°C ambient). The board with the DUT is mounted in a cylindrical enclosure. The power application and signal monitoring are the same as  $\Theta_{JC}$  measurements. The enclosure (ambient) thermocouple is substituted for the fluid thermocouple and two extra thermocouples brought in to monitor room and board temperatures. The junction to ambient thermal resistance is calculated as follows:

$$\Theta_{JA} = (T_J - T_A)/P_d$$

The setup described herein lends itself to the application of various airflow velocities from 0-800 Linear Feet per Minute (LFM), i.e., 0-4.06 m/s. Since the board selection (copper trace density, absence or presence of ground planes, etc.) affects the results of the thermal resistance, the data from these tests shall always be qualified with the board mounting information.

## Data Acquisition and Package Thermal Database

Xilinx gathers data for a package type in die sizes, power levels and cooling modes (air flow and sometimes heatsink effects) with a Data Acquisition and Control system (DAS). The DAS controls the power supplies and other ancillary equipment for hands-free data taking. Different setups within the DAS software are used to run calibration,  $\Theta_{JA}$ ,  $\Theta_{JC}$ , fan tests, as well as the power effect characteristics of a package.

A package is characterized with respect to the major variables that influence the thermal resistance. The results are stored in a database. Thermal resistance data is interpolated as typical values for the individual Xilinx devices that are assembled in the characterized package. Table 3 shows the typical values for different packages. Specific device data may not be the same as the typical data. However, the data will fall within the given minimum and maximum ranges. The more widely used packages will have a wider range. Customers may contact the Xilinx application group for specific device data.

Table 3: Summary of Thermal Resistance for Packages

Package Code	$\Theta_{JA}$ still air (Max)	$\Theta_{JA}$ still air (Typ)	$\Theta_{JA}$ still air (Min)	$\Theta_{JA}$ 250 LFM (Typ)	$\Theta_{JA}$ 500 LFM (Typ)	$\Theta_{JA}$ 750 LFM (Typ)	$\Theta_{Jc}$ (Typ)	Comments
	°C/Watt	°C/Watt	°C/Watt	°C/Watt	°C/Watt	°C/Watt	°C/Watt	
BF957	11.2	10.9	10.6	6.75	5.35	4.6	1.1	2S, 2P, Simulation
BG225	37	30	24	19	17	16	3.3	Various
BG256	32	29	24	19	17	16	3.2	4L/2P-SMT
BG352	14	12	10	8	7	6	0.8	4L/2P-SMT
BG432	13	11	9	8	6	6	0.8	4L/2P-SMT
BG560	10	9	8	7	6	5	0.8	Estimated
BG575	16.9	16.9	16.9	13.7	12.6	11.8	4.7	2S, 2P, Simulation
BG728	13.7	13.5	13.2	10.24	9.3	8.74	2.22	2S, 2P, Simulation
CB100	44	41	38	25	19	17	5.1	Socketed
CB164	29	26	25	17	12	11	3.6	Socketed
CB196	25	24	24	15	11	10	1.8	Socketed
CB228	19	18	17	11	8	7	1.3	Socketed
CS48	-	45	-	-	-	-	-	Estimated
CS144	-	65	-	-	-	-	-	Estimated
DD8	114	109	97	90	73	60	8.2	Socketed
HQ160	14	14	14	10	8	7	1.0	4L/2P-SMT
FF896	11.8	11.8	11.8	8.2	6.7	5.9	1.1	2S, 2P, Simulation
FF1152	11.9	11.65	11.4	7.55	6.05	5.2	1.1	2S, 2P, Simulation
FF1517	10.5	10.5	10.5	6.5	5.1	4.4	1.1	2S, 2P, Simulation
FG256	27	25	23	21	20	19	3.9	4L/2P-SMT
FG456	19	18	17	14	13	13	4.8	4L/2P-SMT
FG556	14	14	14	10	9	9	0.8	4L/2P-SMT
FG676	17	17	17	13	12	12	3.2	4L/2P-SMT
FG680	11	11	10	8	6	6	0.9	4L/2P-SMT
FG860	10	10	10	7	6	5	0.8	4L/2P-SMT
FG900	14	14	14	10	9	9	2.4	Estimated
FG1156	14	13	13	10	9	9	1.85	Estimated
FT256	27.5	29.7	31.9	25.23	23.55	22.8	3.83	2L Substrate, 4L PCB
HQ208	15	14	14	10	8	7	1.7	4L/2P-SMT
HQ240	13	12	12	9	7	6	1.5	4L/2P-SMT
HQ304	11	11	10	7	5	5	0.9	4L/2P-SMT
HT144	-	10.9	-	7.3	5.7	5.0	0.9	4L/2P-SMT
HT176	-	16.0	-	-	-	-	2.0	Estimated
PC20	86	84	76	63	56	53	25.8	2L/0P-SMT
PC44	51	46	42	35	31	29	13.7	2L/0P-SMT

**Table 3: Summary of Thermal Resistance for Packages (Continued)**

Package Code	$\Theta_{JA}$ still air (Max)	$\Theta_{JA}$ still air (Typ)	$\Theta_{JA}$ still air (Min)	$\Theta_{JA}$ 250 LFM (Typ)	$\Theta_{JA}$ 500 LFM (Typ)	$\Theta_{JA}$ 750 LFM (Typ)	$\Theta_{Jc}$ (Typ)	Comments
	°C/Watt	°C/Watt	°C/Watt	°C/Watt	°C/Watt	°C/Watt	°C/Watt	
PC68	46	42	38	31	28	26	9.3	2L/0P-SMT
PC84	41	33	28	25	21	17	5.3	2L/0P-SMT
PD8	82	79	73	60	54	50	22.2	Socketed
PG84	37	34	31	24	18	16	5.8	Socketed
PG120	32	27	25	19	15	13	3.6	Socketed
PG132	32	28	24	20	17	15	2.8	Socketed
PG156	25	23	21	15	11	10	2.6	Socketed
PG175	25	23	20	14	11	10	2.6	Socketed
PG191	24	21	18	15	12	11	1.5	Socketed
PG223	24	20	18	15	12	11	1.5	Socketed
PG299	18	17	16	10	9	8	1.9	Socketed
PG411	16	15	14	9	8	7	1.2	Socketed
PG475	14	13	12	9	8	7	1.2	Socketed
PG559	-	12.00	-	-	-	-	-	Estimated
PP132	35	34	33	23	18	17	6.0	Socketed
PP175	29	29	28	19	15	13	2.5	Socketed
PQ100	35	33	32	29	28	27	5.5	4L/2P-SMT
PQ160	37	32	22	24	21	20	4.6	2L/0P-SMT
PQ208	35	32	26	23	21	19	4.3	2L/0P-SMT
PQ240	28	23	19	17	15	14	2.8	2L/0P-SMT
SO8	147	147	147	112	105	98	48.3	IEEE-(Ref)
TQ100	37	31	31	26	24	23	7.5	4L/2P-SMT
TQ144	35	32	30	25	21	20	5.3	4L/2P-SMT
TQ176	29	28	27	21	18	17	5.3	4L/2P-SMT
VO8	162	162	162	123	116	108	48.3	Estimated
VQ44	44	44	44	36	34	33	8.2	4L/2P-SMT
VQ64	44	41	39	34	32	31	8.2	4L/2P-SMT
VQ100	47	38	32	32	30	29	9.0	4L/2P-SMT



## Application of Thermal Resistance Data

Thermal resistance data is used to gauge the IC package thermal performance. There are several ways to express the thermal resistance between two points. The following are a few of them:

$\theta_{JA}$  = Junction to ambient thermal resistance ( $^{\circ}\text{C}/\text{W}$ ).

$\theta_{JC}$  = Junction to case thermal resistance ( $^{\circ}\text{C}/\text{W}$ )

$\theta_{CA}$  = case to ambient thermal resistance ( $^{\circ}\text{C}/\text{W}$ )

$\theta_{CS}$  = case to heatsink thermal resistance ( $^{\circ}\text{C}/\text{W}$ )

$\theta_{SA}$  = heatsink to ambient thermal resistance ( $^{\circ}\text{C}/\text{W}$ )

$\theta_{JC}$  measures the internal package resistance to heat conduction from the die surface, through the die mount material to the package exterior.  $\theta_{JC}$  strongly depends on the package material's heat conductivity, architecture and geometrical considerations.

$\theta_{JA}$  measures the total package thermal resistance including  $\theta_{JC}$ .  $\theta_{JA}$  depends on the package material properties and such external conditions as convective efficiency and board mount conditions. For example, a package mounted on a socket may have a  $\theta_{JA}$  value 20% higher than the same package mounted on a 4-layer board with power and ground planes.

In general  $\theta_{mn}$  expresses the thermal resistance between point  $m$  and  $n$ . In the above expression the "source" and "end" points are indicated.

In situations where a heatsink is used with a heatsink compound, thermal resistance of heatsink is referenced as  $\theta_{SA}$  (sink-to-ambient) and the attached material as  $\theta_{CS}$  (case-to-heatsink). These thermal resistances may be added. For example,  $\theta_{JC} = \theta_{JA} + \theta_{CS} + \theta_{SA}$  is an expression used in Heatsink situations with interface material resistance  $\theta_{CS}$ .

## Thermal Data Usage

The following are some data requirements for using thermal resistance in an application.

Xilinx supplied data:

$\theta_{JA}$  -- quoted from Xilinx database

$\theta_{JC}$  – quoted from Xilinx database

$\theta_{SA}$  – quoted by heatsink supplier

Items that the user may need to supply.

$T_J$  (max)

This may go as high as the absolute maximum temperature for the package—typically  $125^{\circ}\text{C}$  to  $135^{\circ}\text{C}$  for plastic.

Beyond  $85^{\circ}\text{C}$  for commercial specified part, speed specs may have to be derated. The temperature limit prior to the derating temperature is higher for industrial and military parts.

The user will need to pick a  $T_J$  (max) for reliability considerations, and plan the thermal budget around that.

$T_A$  - Ambient in a system

This is also another variable that the user can control. Typically this is set to around  $45^{\circ}\text{C}$

### Items usually calculated:

Power dissipation. The thermal equation may be used to determine power range that can satisfy some given conditions.

Also if power is known,  $T_J$  (max) may be calculated from the equations.

In non-heatsink situations, the following inequality should hold.

$$T_J (\text{max}) > \theta_{JA} * P_D + T_A$$

The two examples below illustrate the use of the inequality. Specific packages have been used in the examples but any package; Quad, BGA, FGs, or even FlipChip based BGs will be applicable.

### Example 1:

The manufacturer's goal is to achieve  $T_J$  (max)  $< 85^{\circ}\text{C}$

A module is designed for a  $T_A = 45^{\circ}\text{C}$  max.

An XCV300 in a FG456 has a  $\theta_{JA} = 16.5^{\circ}\text{C}/\text{watt}$ .  $\theta_{JC} = 0.8$

Given a XCV300 with a logic design with a rated power  $P_D$  of 2.0 watts.

With this information, the maximum die temperature can be calculated as:

$$T_J = 45 + (16.5 \times 2.0) \implies 78^{\circ}\text{C}.$$

The system manufacturer's goal of  $T_J < 85^{\circ}\text{C}$  is met in this case.

### Example 2:

A module has a  $T_A = 55^{\circ}\text{C}$  max.

The Xilinx FPGA XC4013E is in a PQ240 package (HQ240 is also considered).

A logic design in XC4013E is determined to 2.50 watts. The module manufacturer's goal is to achieve  $T_J$  (max)  $< 100^{\circ}\text{C}$ .

**Table 4** shows the package and thermal enhancement combinations required to meet the goal of  $T_J < 100^{\circ}\text{C}$ .



Table 4: Thermal Resistance for XC4013E in PQ240 and HQ240 Packages

Device Name	Package	$\theta_{JA}$ Still Air	$\theta_{JA}$ (250 LFM)	$\theta_{JA}$ (500 LFM)	$\theta_{JA}$ (750 LFM)	$\theta_{JC}$	Comments
XC4013E	PQ240	23.7	17.5	15.4	14.3	2.7	Cu, SMT 2L/0P
XC4013E	HQ240	12.5	8.6	6.9	6.2	1.5	4-layer board data

**Possible Solutions to meet the module requirements of 100°C :**

- Using the standard PQ240:  $T_J = 55 + (23.7 \times 2.50) \Rightarrow 114.25^\circ\text{C}$ .
- Using standard PQ240 with 250LFM forced air:  $T_J = 55 + (17.5 \times 2.50) \Rightarrow 98.75^\circ\text{C}$ .....
- Using standard HQ240:  $T_J = 55 + (12.5 \times 2.50) \Rightarrow 86.25^\circ\text{C}$ .
- Using HQ240 with 250 LFM forced air:  $T_J = 55 + (8.6 \times 2.50) \Rightarrow 76.5^\circ\text{C}$ .

For all solutions, the junction temperature is calculated as:  $T_J = \text{Power} \times \theta_{JA} + T_A$ . All solutions meet the module requirement of less than 100°C, with the exception of the PQ240 package in still air. In general, depending on ambient and board temperatures conditions, and most importantly the total power dissipation, thermal enhancements—such as forced air cooling, heat sinking, etc., may be necessary to meet the  $T_J$  (max) conditions set.

**Heatsink Calculation**

Example illustrating the use of heatsink:

Device: **XCV1000E-FG680**

There is a need for external thermal enhancements. Supplied data from Xilinx on XCV1000E-FG680:

Table 5: Xilinx Supplied Data

Pkg. Code	$\theta_{JA(0)}$ (°C/W)	$\theta_{JC}$ (°C/W)	$\theta_{JA-250}$ (°C/W)	$\theta_{JA-500}$ (°C/W)	$\theta_{JA-750}$ (°C/W)
FG680	10.6	0.9	7.5	6.1	5.6

Customer requirements:

$T_A = 50^\circ\text{C}$

Power = 8.0 watts (user’s estimate)

User does not want to exceed  $T_J$  (max) of 100°C

Determination with base Still Air data:

$T_J = T_A + (\theta_{JA}) * P$

$T_J = 50 + 8 * 10.6 = 134.8^\circ\text{C}$

Unacceptable!  $\theta_{JA}$  in still air will not work since the 134.8°C is beyond the stated goal of 100°C or less.

Calculating acceptable thermal resistance:

Determine what  $\theta_{JA}$  will be required to stay below 100°C with the 8 watts power?

Thermal budget =  $(T_J - T_A) = 50^\circ\text{C}$ .

$\theta_{JA} = (50)/8 = 6.25^\circ\text{C/Watt}$ .

The package and any enhancement to it needs to have an effective thermal resistance from the junction to ambient less than **6.25°C/Watt**—that becomes the goal any thermal solution ought to meet.

**Solution Options:**

The bare package with 500LFM (2.54 meters/s) of air will give  $\theta_{JA} = 6.1^\circ\text{C/Watt}$  (Table 5). This becomes a workable option if that much airflow can be tolerated.

Heatsink calculation. With a heatsink, heat will now pass through the package ( $\theta_{JC}$ ) then through an interface material ( $\theta_{CS}$ ), and from the heatsink to ambient ( $\theta_{SA}$ ). This can be expressed as follows:

$\theta_{JA} \leq \theta_{JC} + \theta_{CS} + \theta_{SA}$

$6.25 \leq 0.9 + 0.1 + \theta_{SA}$

where

6.25°C/Watt is the condition to be met.

0.9°C/Watt -  $\theta_{JC}$  from data.

0.1°C/Watt -  $\theta_{CS}$  from interface material data.

From above  $\theta_{SA} \leq 5.25^\circ\text{C/Watt}$ .

The objective will be to look for a heatsink with  $\theta_{SA} < 5.25^\circ\text{C/Watt}$  that meets the physical constraints in the system.

Passive heatsink with some air flow: 250LFM (1.25m/s) can be selected.

Active heatsinks: small low profile heatsinks with DC fans may be possible to use.

## PQ/HQ Thermal Data Comparison

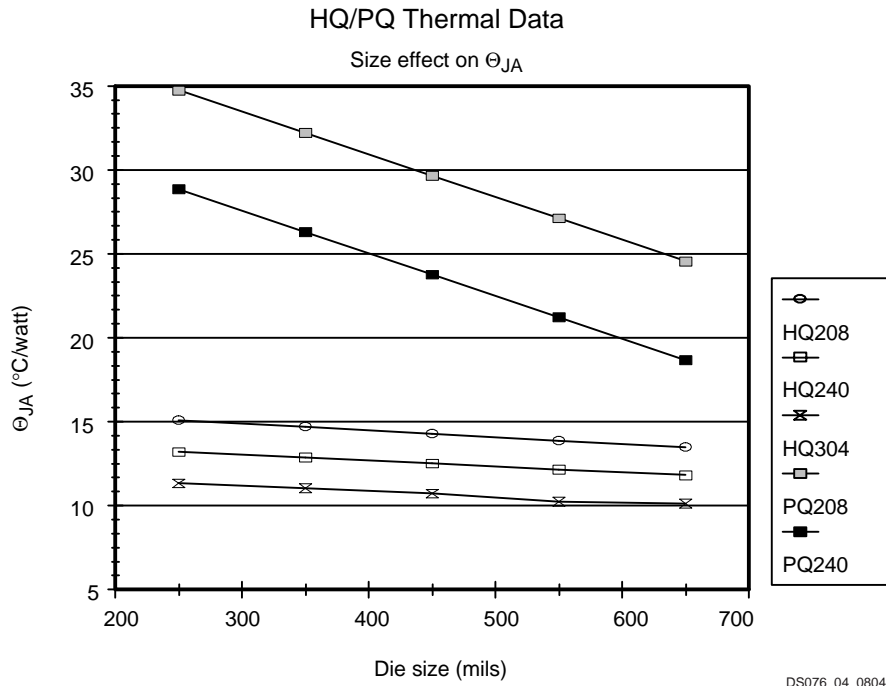


Figure 4: PQ/HQ Thermal Data Comparison

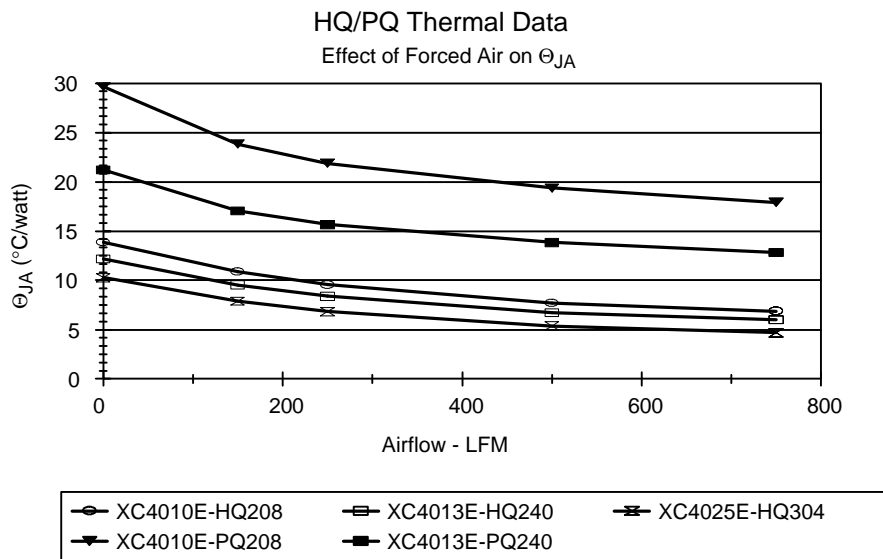


Figure 5: HQ/PQ Thermal Data

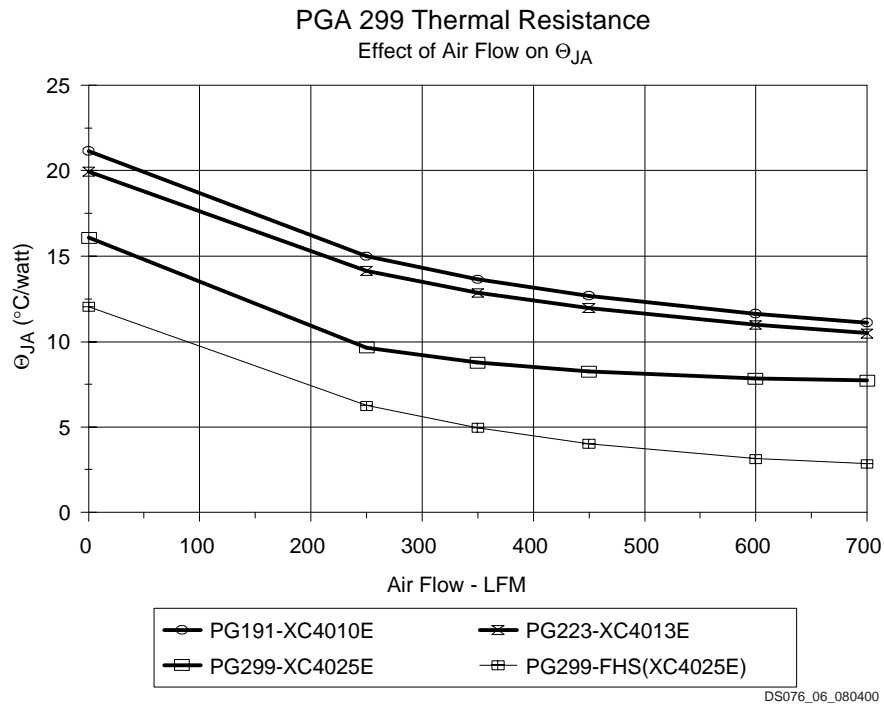


Figure 6: PGA 299 Thermal Resistance

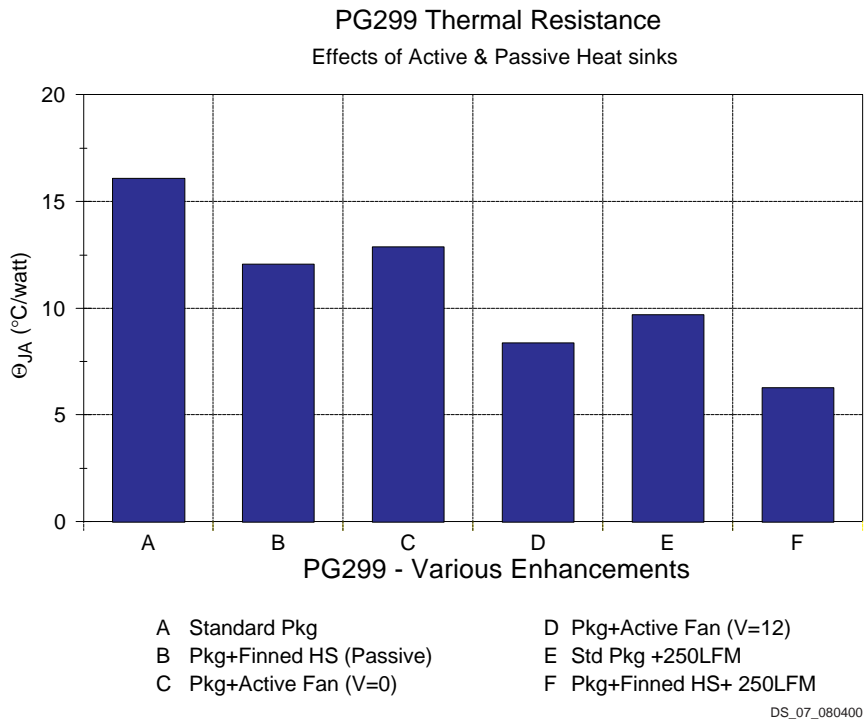


Figure 7: PG299 Thermal Resistance

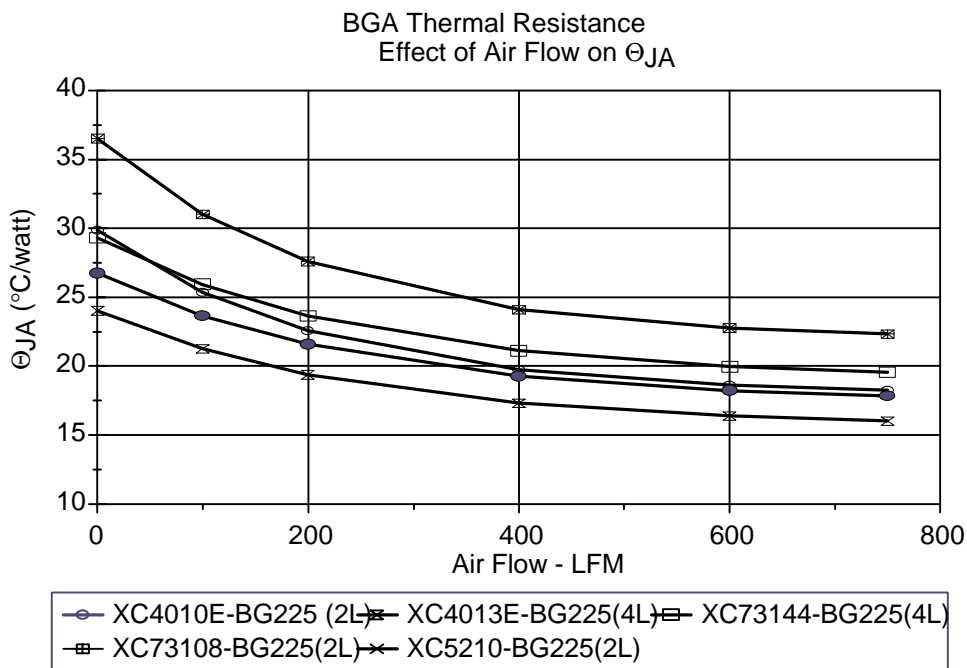


Figure 8: BGA Thermal Resistance

## Some Power Management Options

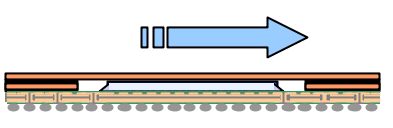
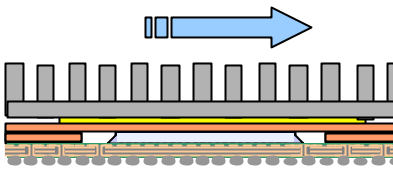
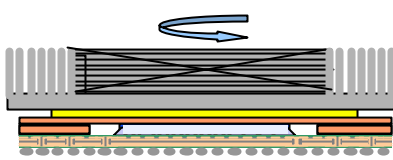


Due to the variety of applications that the FPGA devices are used in, it is a challenge to anticipate the power require-

ments and thus the thermal management needs a particular user may have. While Xilinx programmable devices may not be the dominating power consumers in some systems, it is conceivable to have high gate count FPGA devices exercised sufficiently to generate considerable amount of heat.

In general high I/O and high gate count Virtex class devices stand the potential of being clocked to produce high wattage. Aware of this potential in power needs, the package offering for these devices include medium and high power capable package options. This allows system designer to further enhance these high-end BGA packages to handle more power.

When the actual or estimated power dissipation appears to be more than the specification of the bare package, some thermal management options can be considered. The accompanying Thermal management chart (Figure 9) illustrates the incremental nature of the recommendations—ranging from simple airflow to schemes that can include passive heatsinks, and active heatsinks .

Low End 1-6 Watts	Bare Package with Moderate Air 8-12°C/Watt	Bare Package. Package may be used with moderate airflow within a system.	
Mid Range 4-10 Watts	Passive H/S + Air 5-10°C/Watt	Package used with various forms of Passive Heatsinks and Heat spreader techniques.	
High End 8-20 Watts	Active Heatsink 2-3°C/Watt or better	Package used with Active Heatsinks TEC and Board level Heat spreader techniques.	

DS076\_09\_111200

Figure 9: Thermal Management — Incremental Options

The use of heatpipes, and even liquid-cooled heat plates may be considered in the extreme for some of these packages. Details on the engineering designs and analysis of some of these suggested considerations may require the help of thermal management consultants. The references listed at the end of this section can provide heatsink solutions for industry standard packages.

Some of the options available in thermal management may include the following:

A Xilinx lower voltage version of the equivalent circuit in the same or similar package. With the product and speed grade of choice, up to a 40% power reduction can be anticipated for a 5.0V to a 3.3V version. Not all products have equivalent lower voltage versions.

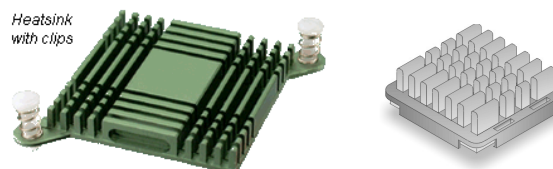
Most high gate count Xilinx devices come in more than two package types. Explore thermally enhanced package options available for the same device. The Quad packages and some BGA packages have heat enhancement options. Typically 25% to 40% improvement in thermal performance can be expected from these heatsink embedded packages.

In a system design, natural convection can be enhanced with venting in the system enclosure. This will effectively lower the  $T_A$ , and increase available thermal budget for moderate power dissipation.

The use of forced air fans will be the next step from the natural convection, and it is an effective way to improve thermal performance. As seen on the graphs and the calculations above, forced air (200-300 LFM) can reduce junction to ambient thermal resistance by up to 30%.

For moderate power dissipation (2 to 5 watts), the use of passive heatsinks and heatspreaders attached with ther-

mally conductive double-sided tapes or retainers can offer quick solutions.



The use of lightweight finned external passive heatsinks can be effective for dissipating up to 8 watts on some packages. If implemented with forced air as well, the benefit can be a 40% to 50% reduction as illustrated in the XCV1000E-FG680 example. The more efficient external heatsinks tend to be tall and heavy. To help prevent component joint from heatsink induced stress the use of spring loaded pins or clips that transfer the mounting stress to a circuit board is advisable whenever a bulky heatsink is considered. The diagonals of some of these heatsinks may be designed (see accompanying picture) with extensions to allow direct connection to the board.

Exposed Metal heatsink packages: All thermally enhanced BGAs with die facing down (including these package codes - BG352, BG432, BG560, FG680, FG860 and FlipChip BGAs) are offered with exposed metal heatsink at the top. These are considered high-end thermal packages and they lend themselves to the application of external heatsinks (passive or active) for further heat removal efficiency. Again precaution should be taken to prevent component damage when a bulky heatsink is attached.

Active heatsinks may include simple heatsink incorporating a mini fan or even Peltier Thermoelectric Cooler (TECs) with a fan to carry away any heat generated. Any consideration to apply TEC in heat management should require consultation with experts in using the device since these devices can

be reversed and cause damage to components. Also condensation can be an issue.



Example of Active Heatsink for BGA(Malico)

Molded packages (FG456, FG676, FG1156, PQs, etc) without exposed metal at the top may also use these heatsinks at the top for further heat reduction. These BGA packages are similar in construction to those used in graphics cards in the PC applications, and heatsinks used for those applications can easily be used for these packages as well. In this case the Junction to Case resistance will be the limiting consideration.

Outside the package itself, the board on which the package sits can have a significant impact on thermal performance. Board designs may be implemented to take advantage of the board's ability to spread heat. Heat flows to the outside of a package and is sunk into the board to be conducted away – through heatpipes or by normal convection. The effect of the board will be dependent on the size and how it conducts heat. Board size, the level of copper traces on it, the number of buried copper planes all lower the junction-to-ambient thermal resistance for a package mounted on it. Some of the heatsink packages – like HQ, with the exposed heatsink on the board side can be glued to the board with thermal compound to enhance heat removal into the board. BGA packages with full matrix of balls can be cooled with this scheme. Users need to be aware that a direct heat path to the board from a component also exposes the component to the effect of other heat sources – particularly if the board is not cooled effectively. An otherwise cooler component can be heated by other heat contributing components on the board.

## References

The following websites have additional information on heat management. The sites carry the contact information:

### Websites for Heatsink Sources

[http:// www.wakefield.com](http://www.wakefield.com)

[http:// www.aavid.com](http://www.aavid.com) or [www.thermalloy.com](http://www.thermalloy.com)

<http://www.chipcoolers.com>

[http:// www.metalsgroup.com](http://www.metalsgroup.com)

<http://www.malico.com.tw>

<http://www.pinfan.com>

[http:// www.intricast.com](http://www.intricast.com)

[http:// www.innovalue.com](http://www.innovalue.com)

<http://www.alphanovatech.com>

[http:// www.tennmax.com](http://www.tennmax.com)

GlobalWin: <http://www.globalwin.com.tw>

<http://www.avc.com.tw>

ALPHA: <http://www.micforg.co.jp>

COFAN USA <http://www.cofan-usa.com>

### Websites for Interface Material Sources

Power Devices - <http://www.powerdevices.com>

Chomerics - <http://www.chomerics.com>

Bergquist Company -

<http://www.bergquistcompany.com>

AOS Thermal Compound - <http://www.aosco.com>

Xilinx does not endorse these vendors nor their products. They are listed here for reference only. Any materials or services received from the vendors should be evaluated for compatibility with Xilinx components.

## Package Electrical Characterization

In high-speed systems, the effects of electrical package parasitics become very critical when optimizing for system performance. Such problems as ground bounce and crosstalk can occur due to the inductance, capacitance, and resistance of package interconnects. In digital systems, such phenomena can cause logic error, delay, and reduced system speed. A solid understanding and proper usage of package characterization data during system design simulation can help prevent such problems.

## Theoretical Background

There are three major electrical parameters which are used to describe the package performance: resistance, capacitance, and inductance. Also known as interconnect parasitics, they can cause many serious problems in digital systems. For example, a large resistance can cause RC and RL off-chip delays, power dissipation, and edge-rate degradation. Large capacitance can cause RC delays,



crosstalk, edge-rate degradation, and signal distortion. The lead inductance, perhaps the most damaging parasitic in digital circuitry, can cause such problems as ground bounce (also known as simultaneous switching noise or delta-I noise), RL delays, crosstalk, edge rate degradation, and signal distortion.

Ground bounce is the voltage difference between any two grounds (typically between an IC and circuit board ground) induced by simultaneously switching current through bondwire, lead, or other interconnect inductance.

When IC outputs change state, large current spikes result from charging or discharging the load capacitance. The larger the load capacitance and faster the rise/fall times, the larger the current spikes are:  $I = C \cdot dv/dt$ . Current spikes through the IC pin and bondwire induces a voltage drop across the leads and bondwires:  $V = L \cdot di/dt$ . The result is a momentary voltage difference between the internal IC ground and system ground, which show up as voltage spikes and unswitched outputs.

Factors that affect ground bounce:

- rise and fall times
- load capacitance
- package inductance
- number of output drivers sharing the same ground path
- device type

## Analytical Formulas for Lead Inductance

1. Rectangular Leadframe/Trace (straight)

$$L_{\text{self}} = 51 \left[ \ln \left( \frac{2l}{w+t} \right) + \frac{1}{2} \right] \text{ nH}$$

(no ground)

$$L_{\text{self}} = 51 \left[ \ln \left( \frac{8h}{w+t} \right) + \left( \frac{w+t}{4h} \right) \right] \text{ nH}$$

(above ground)

$l$  = lead/trace length

$w$  = lead/trace width

$t$  = lead/trace thickness

$h$  = ground height

unit = inches

2. Bondwire (gold wire)

$$L_{\text{wire}} = 51 \left[ \ln \left( \frac{2l}{r} \right) - \frac{3}{4} \right] \text{ nH}$$

$L$  = wire length

$r$  = wire radius

unit = inches

## General Measurement Procedure

Xilinx uses the Time-Domain Reflectometry (TDR) method for parasitic inductance and capacitance measurements. The main components of a TDR setup includes: a digitizing sampling oscilloscope, a fast rise time step generator (<17 ps), a device-under-test (DUT) interface, and an impedance-profile analysis software to extract parasitic models from the TDR reflection waveforms. In this method, a voltage step is propagated down the package under test, and the incident and reflected voltage waves are monitored by the oscilloscope at a particular point on the line. The resulting characteristic impedance of the package interconnect shows the nature (resistive, inductive, and capacitive) of each discontinuity.

### Package and Fixture Preparation

Before performing the measurements, the package and the DUT interface must be fixtured. Proper fixturing ensures accurate and repeatable measurements. The mechanical sample for all inductance (self and mutual) measurements are finished units with all leads shorted to the internal ground. For packages without an internal ground (i.e., QFP, PLCC, etc.) the die-paddle is used instead. The mechanical sample for all capacitance (self and mutual) measurements are finished units with all internal leads floating. The DUT interface provides a physical connection between the oscilloscope and the DUT with minimum crosstalk and probe/DUT reflection. It also provides small ground loop to minimize ground inductance of the fixture.

### Inductance and Capacitance Measurement Procedure

For inductance measurements, a minimum of 25% and maximum of 50% of packages leads, including all leads that are adjacent to the lead(s) under test, are insulated from the DUT fixture ground. All other leads, except for the lead(s) under test, are grounded. This insulation forces the current to return through a low impedance path created on the opposite side of the package. It also eliminates mutual coupling from the neighboring leads. Self-inductance is measured by sending a fast risetime step waveform through the lead under test. The inductive reflection waveform through the lead and the bondwire is then obtained. This reflection waveform, which includes the inductance of the die-paddle (for QFP and PLCC-type packages) and parallel combination of leads in the return path, is the self-inductance. The parasitic effects of the return path are small enough to ignore in the context of this method. For mutual-inductance measurement, two adjacent leads are probed. A fast risetime step waveform is sent through one of the leads. The current travels through the lead/bondwire and returns by the path of the low-impedance ground. On the adjacent "quiet" lead, a waveform is induced due to mutual coupling. This waveform is measured as the mutual inductance.

For capacitance measurements, all external leads except for the lead(s) under test are grounded to the DUT fixture.



For QFP, PLCC, and Power Quad-type of packages, the die-paddle and the heat slug are left floating. Self-capacitance is measured by sending a fast risetime step waveform through the lead under test. The reflection waveform from the lead, which includes the sum of all capacitive coupling with respect to the lead under test, is then measured. Appropriately, the self-capacitance can also be called the “bulk” capacitance since the measured value includes the capacitance between the lead under test and all surrounding metal, including the ground plane and the heat slug. For mutual-capacitance measurement, two adjacent leads are probed. An incident waveform is sent through one lead, and the induced waveform on the neighboring lead is measured as the mutual capacitance.

In order to de-embed the electrical parasitics of the DUT fixture and the measuring probes, the short and the open compensation waveforms are also measured after each package measurement. This procedure compensates the DUT fixture to the very tip of the probes.

### ***Inductance and Capacitance Model Extraction***

All measured reflection waveforms are downloaded to a PC running the analysis software for package parasitic model

extraction. The software uses a method called the Z-profile algorithm, or the impedance-profile algorithm, for parasitic analysis. This method translates the downloaded reflection waveforms into true impedance waveforms, from which package models for inductance and capacitance are extracted.

### **Data Acquisition and Package Electrical Database**

Xilinx acquires electrical parasitic data only on the longest and the shortest lead/traces of the package. This provides the best and the worst case for each package type (defined by package design, lead/ball count, pad size, and vendor). For convenience, the corner interconnects are usually selected as the longest interconnect, while the center interconnects are usually selected as the shortest.

For symmetrical quad packages, all four sides of the package are measured and averaged. Three to five samples are usually measured for accuracy and continuity purposes. The average of these samples is then kept as the official measured parasitic data of that package type in the database.

## Component Mass (Weight) by Package Type

Package	Description	JEDEC Outline #	Xilinx #	Mass (g)
BF957	957 BALL- FLIP CHIP BGA 40 X 40 BODY (1.27mm PITCH)	MS-034-BAU-1 (DEPOPULATED)	OBG0036	18.49
BG225	MOLDED BGA 27 mm FULL MATRIX	MO-151-CAL	OBG0001	2.2
BG256	MOLDED BGA 27 mm SQ	MO-151-CAL	OBG0011	2.2
BG352	SUPERBGA - 35 X 35 mm PERIPHERAL	MO-151-BAR	OBG0008	7.1
BG432	SUPERBGA - 40 X 40 mm PERIPHERAL	MO-151-BAU	OBG0009	9.1
BG492	MOLDED BGA - 35mm-1.27mm Pitch	MO-151-BAR	OBG0026	5.0
BG560	SUPERBGA - 42.5 X 42.5 mm SQ	MO-192-BAV	OBG0010	11.5
BG575	575 BGA 31 X 31mm BODY (1.27mm PITCH)	MS-034-BAN-1 (DEPOPULATED)	OBG0039	4.58
BG728	728 BGA 35 X 35mm BODY (1.27mm PITCH)	MS-034-BAR-1	OBG0030	6.2
CB100	NCTB TOP BRAZE 3K VER	MO-113-AD <sup>(3)</sup>	OCQ0008	10.8
CB100	NCTB TOP BRAZE 4K VER	MO-113-AD <sup>(3)</sup>	OCQ0006	10.8
CB164	NCTB TOP BRAZE 3K VER	MO-113-AA-AD <sup>(3)</sup>	OCQ0003	11.5
CB164	NCTB TOP BRAZE 4K VER	MO-113-AA-AD <sup>(3)</sup>	OCQ0007	11.5
CB196	NCTB TOP BRAZE 4K VER	MO-113-AB-AD <sup>(3)</sup>	OCQ0005	15.3
CB228	NCTB TOP BRAZE 4K VER	MO-113-AD <sup>(3)</sup>	OCQ0012	17.6
CC20	CERAMIC LEADED CHIP CARRIER	NA	OCQ0011	8.4
CC44	CERAMIC LEADED CHIP CARRIER	MO-087	OCQ0013	2.9
CD48	CERAMIC SIDEBRAZED - DIP	NA	OPD0004	8.0
CD8	CERAMIC SIDEBRAZED - DIP	NA	OPD0003	0.9
CG1156	CERAMIC - HiTCE BGA - 35sq. 1.0mm	MO-151	OBG0031	0.0
CG225	CERAMIC DIMPLED BGA	NA	OBG0002	5.9
CP56	CSP 56 BGA - 6mm (0.5 pitch)	NA	OBG0029	0.0
CQ100	CERQUAD UNFORMED	MO-082-AC	OCQ0001	3.6
CS48	CSP 48 BGA - 7mm (0.8mm pitch)	MO-195	OBG0012	0.2
CS144	CSP 144 BGA - 12mm (0.8mm pitch)	MO-205-BE	OBG0015	0.3
CS280	CSP 280 BGA - 16mm (0.8mm pitch)	MO-205-AH	OBG0024	0.0
DD8	.300 CERDIP PACKAGE	MO-036-AA	OPD0005	1.1
FF896	896 BALL - FLIP CHIP BGA 31 X 31mm BODY (1.0mm PITCH)	MS-034-AAN-1	OBG0032	10.7
FF1152	1152 BALL - FLIP CHIP BGA 35 X 35mm BODY (1.0mm PITCH)	MS-034-AAR-1 (DEPOPULATED)	OBG0033	14.24
FF1517	1517 BALL - FLIP CHIP BGA 40 X 40mm BODY (1.0mm PITCH)	MS-034-AAU-1 (DEPOPULATED)	OBG0034	18.53
FG256	Fine Pitch BGA 17 x 17 mm, 1.0 mm ball pitch	MO-151-AAF-1	OBG0021	0.8
FG456	Fine Pitch BGA 23 x 23 mm, 1.0 mm ball pitch	MO-151-AAJ-1	OBG0019	2.1
FG556	Fine Pitch BGA 31 x 31 mm, 1.0 mm ball pitch	MO-151-AAN-1	OBG0020	3.92
FG676	Fine Pitch BGA, 27 x 27 mm, 1.0 mm ball pitch	MO-151-AAL-1	OBG0018	3.3
FG680	Fine Pitch BGA 40 x 40 mm, 1.0 mm ball pitch	MO-151-AAU-1	OBG0022	10.3
FG900	Fine Pitch BGA, 31 x 31 mm, 1.0 mm ball pitch	MO-151-AAN-1	OBG0027	4.0
FG1156	Fine Pitch BGA, 35 x 35 mm, 1.0 mm ball pitch	MO-151-AAR-1	OBG0028	5.5

## Component Mass (Weight) by Package Type (Continued)

Package	Description	JEDEC Outline #	Xilinx #	Mass (g)
FT256	256 THIN PBGA 17 X 17mm BODY (1.0mm PITCH)	MS-034-AAF-1 (EXCEPT FOR THE SIZE OF THE BALL		
HQ160	METRIC 28 28-0.65 mm 1.6H/S DIE UP	MO-108-DDI	OPQ0021	10.8
HQ208	METRIC 28 X 28-H/S DIE UP	MO-143-FA1	OPQ0020	10.8
HQ240	METRIC QFP 32 32-H/S DIE UP	MO-143-GA	OPQ0019	15.0
HQ304	METRIC QFP 40 40-H/S DIE DOWN	MO-143-JA	OPQ0014	26.2
HT144	THIN QFP 1.4 H/S (HQ) DIE UP	MS-026-BFB	OPQ0025	2.6
HT176	THIN QFP 1.4 H/S (HQ) DIE UP	MS-026-BGA	OPQ0026	3.5
HT208	THIN QFP 1.4 H/S (HQ) DIE UP	MS-026-BJB	OPQ0027	4.3
MQ208	28X28 METAL QUAD EIAJ OUTLINE	NA	OPQ0006	6.1
MQ240	32X32 METAL QUAD EIAJ OUTLINE	NA	OPQ0011	8.0
PC20	PLCC JEDEC MO-047	MO-047-AA	OPC0006	0.8
PC28	PLCC JEDEC MO-047	MO-047-AB	OPC0001	1.1
PC44	PLCC JEDEC MO-047	MO-047-AC	OPC0005	1.2
PC68	PLCC JEDEC MO-047	MO-047-AE	OPC0001	4.8
PC84	PLCC JEDEC MO-047	MO-047-AF	OPC0001	6.8
PD8	DIP .300 STANDARD	MO-001-AA	OPD0002	0.5
PD48	DIP .600 STANDARD	NA	OPD0001	7.9
PG68	CERAMIC PGA CAVITY UP 11 X 11	MO-067-AC	OPG0002	7.0
PG84	CERAMIC PGA CAVITY UP 11 X 11	MO-067-AC	OPG0003	7.2
PG84	WINDOWED CPGA CAVITY UP 11 X 11	MO-067-AC	OPG0013	7.5
PG120	CERAMIC PGA 13 X 13 MATRIX	MO-067-AE	OPG0012	11.5
PG132	CERAMIC PGA 14 X 14 MATRIX	MO-067-AF	OPG0004	11.8
PG144	CERAMIC PGA 15 X 15 CAVITY UP	MO-067-AG	OPG0017	16.9
PG156	CERAMIC PGA 16 X 16 MATRIX	MO-067-AH	OPG0007	17.1
PG175	CERAMIC PGA 16 X 16 STD VER.	MO-067-AH	OPG0009	17.7
PG191	CERAMIC PGA 18 X 18 STD - ALL	MO-067-AK	OPG0008	21.8
PG223	CERAMIC PGA 18 X 18 TYPE	MO-067-AK	OPG0016	26.0
PG299	CERAMIC PGA 20 X 20 HEATSINK	MO-067-AK	OPG0022	37.5
PG299	CERAMIC PGA 20 X 20 TYPE	MO-067-AK	OPG0015	29.8
PG411	CERAMIC PGA 39 X 39 STAGGER	MO-128-AM	OPG0019	36.7
PG475	CERAMIC PGA 41 X 41 STAGGER	MO-128-AM	OPG0023	39.5
PG559	CERAMIC PGA 43 x 43	MO-128	OPG0025	44.50
PP132	PLASTIC PGA 14 X 14 MATRIX	MO-83-AF	OPG0001	8.1
PP175	PLASTIC PGA 16 X 16 BURIED	MO-83-AH	OPG0006	11.1
PQ44	EIAJ 10 X 10 X 2.0 QFP	MS-022-AB	OPQ0015	0.5
PQ100	EIAJ 14 X 20 QFP - 1.60 (DEFAULT)	MO-108-CG1	OPQ0013	1.6
PQ100	EIAJ 14 X 20 QFP - 1.80 (NOT USED)	EIAJ-OLD	OPQ0016	1.6
PQ100	EIAJ 14 X 20 QFP - 1.95 (OLD VERSION)	MO-108-CC2	OPQ00013	1.6
PQ160	EIAJ 28 X 28 0.65 mm 1.60	MO-108-DD1	OPQ0002	5.8
PQ208	EIAJ 28 X 28 0.5 mm 1.30	MO-143-FAI	OPQ0003	5.3
PQ240	EIAJ 32 X 32 0.5 mm	MO-143-GA	OPQ0010	7.1

## Component Mass (Weight) by Package Type (Continued)

Package	Description	JEDEC Outline #	Xilinx #	Mass (g)
SO8	VERSION 1 - 0.150/55MIL	MO-150	OPD0006	0.1
SO20	300 MIL SOIC	MS-103	OPD0009	0.5
SO24	300 MIL SOIC	MS-013	OPD0010	0.6
TQ100	THIN QFP 1.4 mm thick	MS-026-BDE	OPQ0004	0.7
TQ128	THIN QFP 1.4 mm thick - RECT	MS-026-BHB	OPQ0028	0.8
TQ144	THIN QFP 1.4 mm thick	MS-026-BFB	OPQ0007	1.4
TQ176	THIN QFP 1.4 mm thick	MS-026-BGA	OPQ0008	1.9
VO8	THIN SOIC-II	N/A	OPD0007	0.1
VQ100	THIN QFP 1.0 thick	MS-026-AED	OPQ0012	0.6
VQ44	THIN QFP 1.0 thick	MS-026-ACB	OPQ0017	0.4

### Notes:

1. Data represents average values for typical packages with typical devices. The accuracy is between 7% to 10%.
2. More precise numbers (below 5% accuracy) for specific devices may be obtained from Xilinx through a factory representative or by calling the Xilinx Hotline.
3. Tie-bar details are specific to Xilinx package. Lead width minimum is 0.056".

## Xilinx Thermally Enhanced Packaging

### The Package Offering

Xilinx Code	Body (mm)	THK (mm)	Mass (gm)	Heatsink Location	JEDEC No.	Xilinx No.
HQ160	28x28	3.40	10.8	DOWN	MO-108-DD1	OPQ0021
HQ208	28x28	3.40	10.0	DOWN	MO-143-FA	OPQ0020
HQ240	32x32	3.40	15.0	DOWN	MO-143-GA	OPQ0019
HQ304	40x40	3.80	26.2	TOP	MO-143-JA	OPQ0014

## Overview

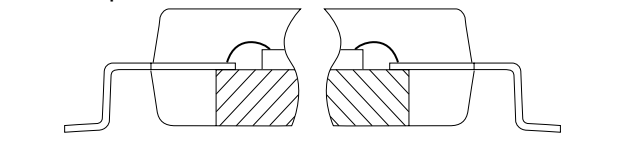
Xilinx offers thermally enhanced quad flat pack packages on certain devices. This section discusses the performance and usage of these packages (designated HQ). In summary:

- The HQ-series and the regular PQ packages conform to the same JEDEC drawings.
- The HQ and PQ packages use the same PCB land patterns.
- The HQ packages have more mass
- Thermal performance is better for the HQ packages

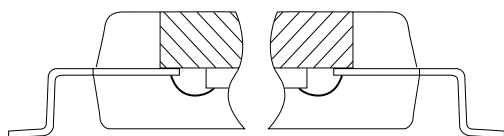
## Where and When Offered

- HQ packages are offered as the thermally enhanced equivalents of PQ packages. They are used for high gate count or high I/O count devices in packages, where heat dissipation without the enhancement may be a handicap for device performance. Such devices include XC4013E, XC4020E, XC4025E, and XC5215.
- They are also being used in place of MQUAD (MQ) packages of the same lead count for new devices.
- The HQ series at the 240-pin count level or below are offered with the heatsink at the bottom of the package. This was done to ensure pin to pin compatibility with the existing PQ and MQ packages.
- At the 304-pin count level, the HQ is offered with the heatsink up. This arrangement offers a better potential for further thermal enhancement by the designer.

### A Die Up/Heatsink Down



### B Die Down/Heatsink Up



A – Heatsink down orientation

B – Heatsink up orientation

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Figure 10: Heatsink Orientation

## Mass Comparison

Because of the copper heatsink, the HQ series of packages are about twice as heavy as the equivalent PQ. Here is a quick comparison.

	HQ (gm)	PQ (gm)
160-pin	10.8	5.8
208-pin	10.8	5.3
240-pin	15.0	7.1
304-pin	26.2	N/A

## Thermal Data for the HQ

The data for individual devices may be obtained from Xilinx.

Still Air Data Comparison		
	HQ $\Theta_{JA}$ (°C/Watt)	PQ $\Theta_{JA}$ (°C/Watt)
160-pin	13.5-14.5	20.5-38.5
208-pin	14-15	26-35
240-pin	12-13	19-28
304-pin	10-11	N/A

### Notes:

1.  $\Theta_{JC}$  is typically between 1 and 2°C/Watt for HQ and MQ Packages. For PQ's, it is between 2 and 7°C/Watt.

Data Comparison at Airflow - 250 LFM		
	HQ $\Theta_{JA}$ (°C/Watt)	PQ $\Theta_{JA}$ (°C/Watt)
160-pin	9-10	15-28.5
208-pin	9-10	14-26
240-pin	8-9	11-21
304-pin	6.5-8	N/A

## Other Information

- Leadframe: Copper EFTEC-64 or C7025
- Heat Slug: Copper - Nickel plated → Heatsink metal is Grounded
- Lead Finish 85/15 Sn/Pb 300 microinches minimum
- D/A material: Same as PQ; Epoxy 84-1LMISR4
- Mold Cpd: Same as PQ - EME7304LC
- Packed in the same JEDEC trays

## Moisture Sensitivity of PSMCs

### Moisture Induced Cracking During Solder Reflow

The surface mount reflow processing step subjects the Plastic Surface Mount Components (PSMC) to high thermal exposure and chemicals from solder fluxes and cleaning fluids during user's board mount assembly. The plastic mold compounds used for device encapsulation are, universally, hygroscopic and absorb moisture at a level determined by storage environment and other factors. Entrapped moisture can vaporize during rapid heating in the solder reflow process generating internal hydrostatic pressure. Additional stress is added due to thermal mismatch, and the Thermal Coefficient of Expansion (TCE) of plastic, metal lead frame, and silicon die. The resultant pressure may be sufficient to cause delamination within the package, or worse, an internal or external crack in the plastic package. Cracks in the plastic package can allow high moisture penetration, inducing transport of ionic contaminants to the die surface and increasing the potential for early device failure.

How the effects of moisture in plastic packages and the critical moisture content result in package damage or failure is a complex function of several variables. Among them are package construction details—materials, design, geometry, die size, encapsulant thickness, encapsulant properties, TCE, and the amount of moisture absorbed. The PSMC moisture sensitivity has, in addition to package cracking, been identified as a contributor to delamination-related package failure artifacts. These package failure artifacts include bond lifting and breaking, wire neckdown, bond cratering, die passivation, and metal breakage.

Because of the importance of the PSMC moisture sensitivity, both device suppliers and device users have ownership and responsibility. The background for present conditions,

moisture sensitivity standardized test and handling procedures have been published by two national organizations. Users and suppliers are urged to obtain copies of both documents (listed below) and use them rigorously. Xilinx adheres to both.

- JEDEC STANDARD JESD22-A112. Test Method A112 “Moisture-Induced Stress Sensitivity for Plastic Surface Mounted Devices”. Available through Global Engineering Documents Phone: USA and Canada 800-854-7179, International 1-303-792-2181
- IPC Standard IPC-SM-786A “Procedures for Characterizing and Handling of Moisture/Reflow Sensitive ICs”. Available through IPC Phone: 1-708-677-2850

None of the previously stated or following recommendations apply to parts in a socketed application. For board mounted parts careful handling by the supplier and the user is vital. Each of the above publications has addressed the sensitivity issue and has established six levels of sensitivity (based on the variables identified). A replication of those listings, including the preconditioning and test requirements, and the factory floor life conditions for each level are outlined in **Table 6**. Xilinx devices are characterized to their proper level as listed. This information is conveyed to the user via special labeling on the Moisture Barrier Bag (MBB).

In **Table 6**, the level number is entered on the MBB prior to shipment. This establishes the user's factory floor life conditions as listed in the time column. The soak requirement is the test limit used by Xilinx to determine the level number. This time includes manufacturer's exposure time or the time it will take for Xilinx to bag the product after baking.

**Table 6: Package Moisture Sensitivity Levels per J-STD-020**

Level	Factory Floor Life		Soak Requirements (Preconditioning)			
	Conditions	Time	Time			Conditions
1	≤30°C / 90% RH	Unlimited	168 hours			85°C / 85% RH
2	≤30°C / 60% RH	1 year	168 hours			85°C / 60% RH
			Time (hours)			
			X +	Y =	Z	
3	≤30°C / 60% RH	168 hours	24	168	192	30°C / 60% RH
4	≤30°C / 60% RH	72 hours	24	72	96	30°C / 60% RH
5	≤30°C / 60% RH	24/28 hours	24	24/48	48/72	30°C / 60% RH
6	≤30°C / 60% RH	6 hours	0	6	6	30°C / 60% RH

**Notes:**

1. X = Default value of semiconductor manufacturer's time between bake and bag. If the semiconductor manufacturer's actual time between bake and bag is different from the default value, use the actual time.
2. Y = Floor life of package after it is removed from dry pack bag.
3. Z = Total soak time for evaluation.



## Factory Floor Life

Factory floor life conditions for Xilinx devices are clearly stated on MBB containing moisture sensitive PSMCs. These conditions have been ascertained by following Test Methods outlined in JEDEC JESD22-A112 and are replicated in Table 6. If factory floor conditions are outside the stated environmental conditions (30°C/90% RH for Level 1, and 30°C/60% RH for Levels 2-6) or if time limits have been exceeded, then recovery can be achieved by baking the devices before the reflow step. Identified in the next section are two acceptable bake schedules. Either can be used for recovery to the required factory floor level.

## Dry Bake Recommendation and Dry Bag Policy

Xilinx recommends, as do the mentioned publications and other industry studies, that all moisture sensitive PSMCs be baked prior to use in surface mount applications, or comply strictly with requirements as specified on the MBB. Tape and Reeled parts are universally dry packed. Level 1 parts are shipped without the need for, or use of, an MBB.

Two bake schedules have been identified as acceptable and equivalent. The first is 24 hours in air at 125°C, in shipping media capable of handling that temperature. The second bake schedule is for 192 hours in a controlled atmosphere of 40°C, equal to or less than 5% RH.

Dry Devices are sealed in special military specification Moisture Barrier Bags (MBB). Enough desiccant pouches are enclosed in the MBB to maintain contents at less than 20% RH for up to 12 months from the date of seal. A reversible Humidity Indicator Card (HIC) is enclosed to monitor the internal humidity level. The loaded bag is then sealed shut under a partial vacuum with an impulse heat sealer.

Artwork on the bags provides storage, handling and use information. There are areas to mark the seal date, quantity, and moisture sensitivity level and other information. The following paragraphs contain additional information on handling PSMCs.

## Handling Parts in Sealed Bags

### Inspection

Note the seal date and all other printed or hand entered notations. Review the content information against what was ordered. Thoroughly inspect for holes, tears, or punctures that may expose contents. Xilinx strongly recommends that the MBB remain closed until it reaches the actual work station where the parts will be removed from the factory shipping form.

### Storage

The sealed MBB should be stored, unopened, in an environment of not more than 90% RH and 40°C. The enclosed HIC is the only verification to show if the parts have been

exposed to moisture. Nothing in part appearance can verify moisture levels.

### Expiration Date

The seal date is indicated on the MBB. The expiration date is 12 months from the seal date. If the expiration date has been exceeded or HIC shows exposure beyond 20% upon opening the bag bake the devices per the earlier stated bake schedules. The three following options apply after baking:

Use the devices within time limits stated on the MBB.

Reseal the parts completely under a partial vacuum with an impulse sealer (hot bar sealer) in an approved MBB within 12 hours, using fresh desiccant and HIC, and label accordingly. Partial closures using staples, plastic tape, or cloth tape are unacceptable.

Store the out-of-bag devices in a controlled atmosphere at less than 20% RH. A desiccator cabinet with controlled dry air or dry nitrogen is ideal.

### Other Conditions

Open the MBB when parts are to be used. Open the bag by cutting across the top as close to the seal as possible. This provides room for possible resealing and adhering to the reseal conditions outlined above. After opening, strictly adhere to factory floor life conditions to ensure that devices are maintained below critical moisture levels.

Bags opened for less than one hour (strongly dependent on environment) may be resealed with the original desiccant. If the bag is not resealed immediately, new desiccant or the old one that has been dried out may be used to reseal, **if the factory floor life has not been exceeded**. Note that factory floor life is cumulative. Any period of time when MBB is opened must be added to all other opened periods.

Both the desiccant pouches and the HIC are reversible. Restoration to dry condition is accomplished by baking at 125°C for 10-16 hours, depending on oven loading conditions.

## Tape and Reel

Xilinx offers a tape and reel packing for PLCC, BGA, QFP, and SO packages. The packing material is made of black conductive Polystyrene and protects the packages from mechanical and electrical damage. The reel material provides a suitable medium for pick and place equipment.

The tape and reel packaging consists of a pocketed carrier tape, sealed with a protective cover. The device sits on pedestals (for PLCC, QFP packages) to protect the leads from mechanical damage. All devices loaded into the tape carriers are baked, lead scanned before the cover tape is attached and sealed to the carrier. In-line mark inspection for mark quality and package orientation is used to ensure shipping quality.



## Benefits

- Increased quantity of devices per reel versus tubes improves cycle time and reduces the amount of time to index spent tubes.
- Tape and reel packaging enables automated pick and place board assembly.
- Reels are uniform in size enabling equipment flexibility.
- Transparent cover tape allows device verification and orientation.
- Anti-static reel materials provides ESD protection.
- Carrier design include a pedestal to protect package leads during shipment.
- Bar code labels on each reel facilitate automated inventory control and component traceability.
- All tape and reel shipments include desiccant pouches and humidity indicators to insure products are safe from moisture.
- Compliant to Electronic Industries Association (EIA) 481.

## Material and Construction

### Carrier Tape

- The pocketed carrier Tape is made of conductive polystyrene material, or equivalent, with a surface resistivity level of less than 106 ohms per square inch.
- Devices are loaded "live bug" or leads down, into a device pocket.
- Each carrier pocket has a hole in the center for automated sensing of whether a unit is in the pocket or not.
- Sprocket holes along the edge of the carrier tape enable direct feeding into an automated board assembly equipment.

### Cover Tape

- An anti-static, transparent, polyester cover tape, with heat activated adhesive coating, sealed to the carrier edges to hold the devices in the carrier pockets.
- Surface resistivity on both sides is less than 1011 ohms per square inch.

### Reel

- The reel is made of anti-static Polystyrene material. The loaded carrier tape is wound onto this conductive plastic reel.
- A protective strip made of conductive Polystyrene material is placed on the outer part of the reel to protect the devices from external pressure in shipment.
- Surface resistivity is less than 1011 ohms per square inch.
- Device loading orientation is in compliance with EIA Standard 481.

### Bar Code Label

- The bar code label on each reel provides customer identification, device part number, date code of the product and quantity in the reel.
- Print quality are in accordance with ANSI X3.182-1990 Bar Code Print Quality Guidelines. Presentation of Data on labels are EIA-556-A compliant.
- The label is an alphanumeric, medium density Code 39 labels.
- This machine-readable label enhances inventory management and data input accuracy.

### Shipping Box

- The shipping container for the reels are in a 13" x 13" x 3" C-flute, corrugated, #3 white "pizza" box, rated to 200 lb. test.

Table 7: Tape and Reel Packaging

Package Code	Qty. per Reel	Reel Size (inch)	Carrier Width (mm)	Cover Width (mm)	Pitch (mm)
BG225 <sup>(1)</sup>	500	13	44	37,5	32
BG256 <sup>(1)</sup>	500	13	44	37.5	32
BG272 <sup>(1)</sup>	500	13	44	37.5	32
CP56 <sup>(1)</sup>	4,000	13	12	9.2	8
CS48 <sup>(1)</sup>	1,500	13	16	13.3	12
CS144 <sup>(1)</sup>	2,000	13	24	21.0	16
FG256 <sup>(1)</sup>	1,000	13	24	21.0	20
FG456 <sup>(1)</sup>	500	13	44	37.5	32
FG676 <sup>(1)</sup>	500	13	44	37.5	32
PC20 <sup>(1)</sup>	750	13	16	13.3	12
PC44 <sup>(1)</sup>	500	12	32	25.5	24
PC68 <sup>(1)</sup>	250	13	44	37.5	32
PC84 <sup>(1)</sup>	250	13	44	37.5	36

Table 7: Tape and Reel Packaging (Continued)

Package Code	Qty. per Reel	Reel Size (inch)	Carrier Width (mm)	Cover Width (mm)	Pitch (mm)
PQ100	250	13	44	37.5	32
PQ160	200	13	44	37.5	40
SBGA352 <sup>(1)</sup>	200	13	56	49.5	40
SBGA432 <sup>(1)</sup>	200	13	56	49.5	48
SBGA560 <sup>(1)</sup>	200	13	56	49.5	48
SO8	750	7	12	9.2	8
SO20	1,000	13	24	21.0	12
TQ100	1,000	13	24	21.0	32
TQ144	750	13	44	37.5	24
VO8	750	7	12	9.2	8
VQ44	2,000	13	24	21.0	16
VQ64	2,000	13	24	21.0	16
VQ100	1,000	13	24	21.0	32

**Notes:**

1. In-house capability.

### Standard Bar Code Label Locations

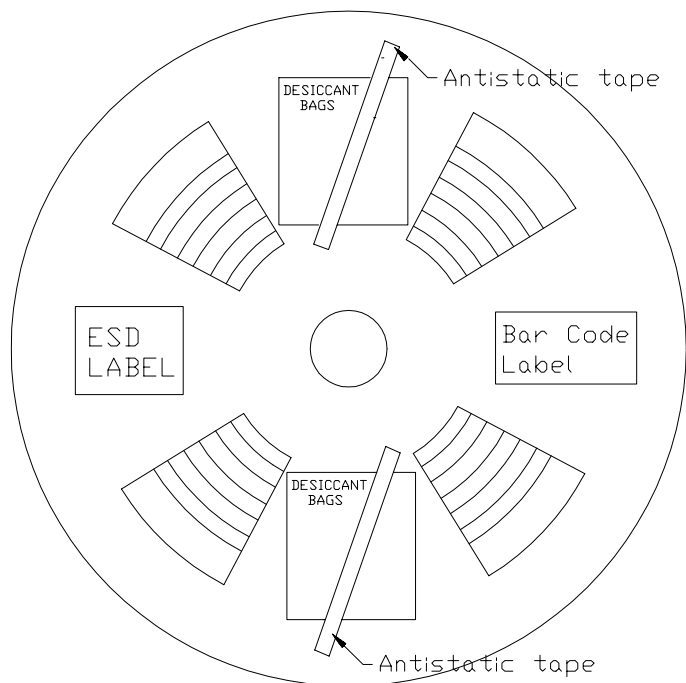


Figure 11: Standard Bar Code Label Locations

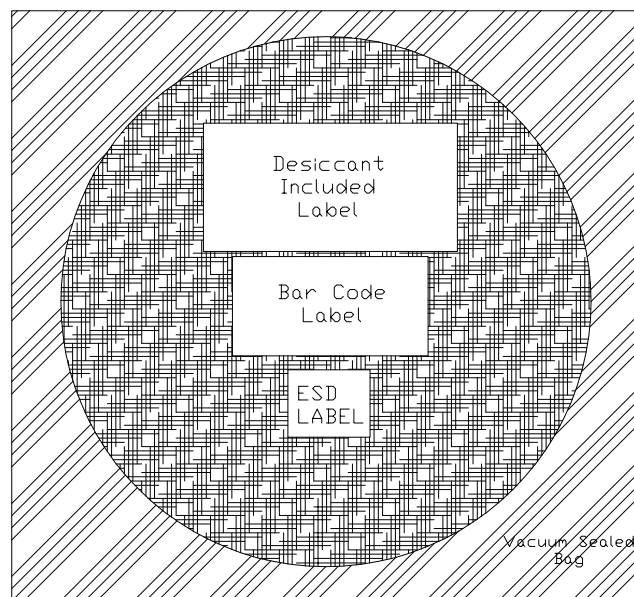


Figure 12: Standard Bar Code Label Locations

### Reflow Soldering Process Guidelines

To implement and control the production of surface mount assemblies, the dynamics of the solder reflow process and how each element of the process is related to the end result must be thoroughly understood.

The primary phases of the reflow process are as follows:

1. Melting the particles in the solder paste
2. Wetting the surfaces to be joined
3. Solidifying the solder into a strong metallurgical bond

The sequence of five actions that occur during this process

is shown in Figure 13.

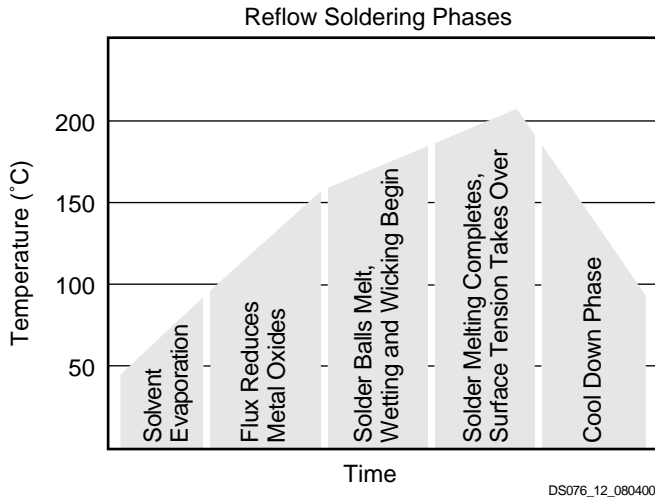
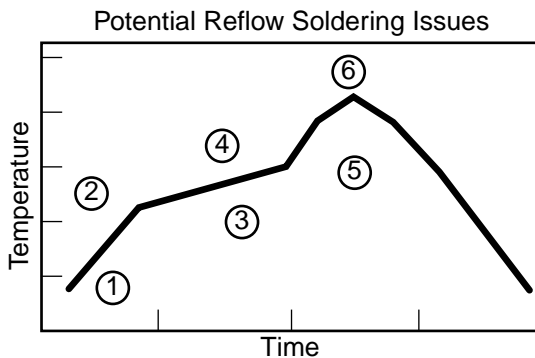


Figure 13: Soldering Sequence

Each phase of a surface mount reflow profile has min/max limits that should be viewed as a process window. The process requires a careful selection and control of the materials, geometries of the mating surfaces (package footprint vs. PCB land pattern geometries) and the time temperature of the profile. If all of the factors of the process are sufficiently optimized, there will be good solder wetting and fillet formation (between component leads and the land patterns on the substrate). If factors are not matched and optimized there can be potential problems as summarized in Figure 14.

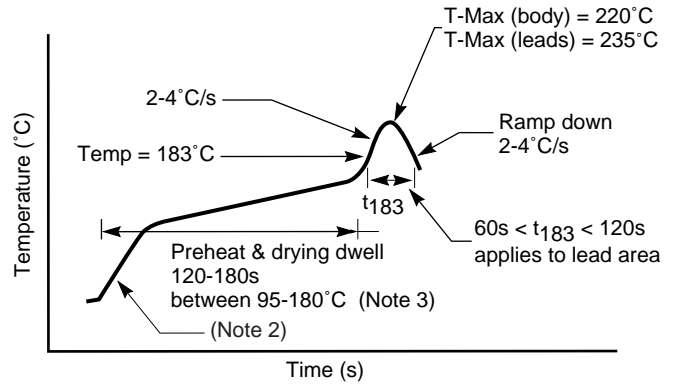


1. Insufficient Temperature to Evaporate Solvent
2. Component Shock and Solder Splatter
3. Insufficient Flux Activation
4. Excessive Flux Activity and Oxidation
5. Trapping of Solvent and Flux, Void Formation
6. Component and/or Board Damage

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Figure 14: Soldering Problems Summary

Figure 15 and Figure Notes: show typical conditions for solder reflow processing using IR/Convection or Vapor Phase. Both IR and Convection furnaces are used for BGA assembly. The moisture sensitivity of Plastic Surface Mount Components (PSMCs) must be verified prior to surface mount flow. See the preceding sections for a more complete discussion on PSMC moisture sensitivity.



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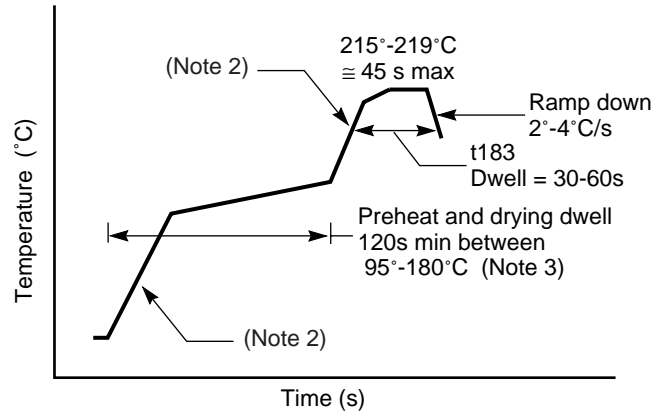
Notes:

1. Max temperature range = 220°C-235°C (leads)  
Time at temp 30-60 seconds
2. Preheat drying transition rate 2-4°C/s
3. Preheat dwell 95-180°C for 120-180 seconds
4. IR reflow shall be performed on dry packages

The IR process is strongly dependent on equipment and loading differences. Components may overheat due to lack of thermal constraints. Unbalanced loading may lead to significant temperature variation on the board. This guideline is intended to assist users in avoiding damage to the components; the actual profile should be determined by the users using these guidelines.

Figure 15: Typical Conditions for IR Reflow Soldering

The peak reflow temperature of the PSMC body should not be more than 220°C in order to avoid internal package delamination. For multiple BGAs in a single board, it is recommended to check all BGA sites for varying temperatures because of differences in surrounding components.



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**Notes:**

1. Solvent - FC5312 or equivalent - ensures temperature range of leads @ 215-219°C
2. Transition rate 4-5°C/s
3. Dwell is intended for partial dryout and reduces the difference in temperature between leads and PCB land patterns.
4. These guidelines are for reference. They are based on laboratory runs using dry packages. It is recommended that actual packages with known loads be checked with the commercial equipment prior to mass production.

**Figure 16: Typical Conditions for Vapor Phase Reflow Soldering**

## Sockets

**Table 8** lists manufacturers known to offer sockets for Xilinx Package types. This summary does not imply an endorse-

ment by Xilinx. Each user has the responsibility to evaluate and approve a particular socket manufacturer.

**Table 8: Socket Manufacturers**

Manufacturer	Packages					
	DIP SO VO	PC WC	PQ HQ TQ VQ	PG PP	CB	BG CG
AMP Inc. 470 Friendship Road Harrisburg, PA 17105-3608 (800) 522-6752	X	X		X		
Augat Inc. 452 John Dietsch Blvd. P.O. Box 2510 Attleboro Falls, MA 02763-2510 (508) 699-7646	X	X		X		
McKenzie Socket Division 910 Page Avenue Fremont, CA 94538 (510) 651-2700	X	X		X		
3M Textool 6801 River Place Blvd. Austin, TX 78726-9000 (800) 328-0411 (612) 736-7167				X	X	X
Wells Electronics 1701 South Main Street South Bend, IN 46613-2299 (219) 287-5941				X		
Yamaichi Electronics Inc. 2235 Zanker Road San Jose, CA 95131 (408) 456-0797		X	X	X	X	

## Revision History

The following table shows the revision history for this document.

Date	Version	Revision
11/13/00	2.2	Specifications updated and added data sheet number.
05/15/01	3.0	Updated all Tables and specification.