White Papers by Product

Virtex Series

Listed below are the Virtex Series White Papers listed by the most recent paper.
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WP140 **Physical Synthesis (v1.0) 02/26/01 (32 KB)** FPGAs

In the domain of deep submicron (DSM) and nanometer ASIC technologies (180 nm and below), the traditional separation between logical (synthesis) and physical (place and route) design methods often causes a problem—designs cannot meet their realistic timing objectives; creating the well known “timing closure problem.“ Timing closure is now considered the biggest area of difficulty for ASIC performance-oriented designs. The underlying reason is that circuit delays are dominated by net delays, which are influenced by the placement of the cells. The traditional fanout-based wireload models, for estimating interconnect delay during synthesis, are considered inaccurate and are the key factor causing the lack of timing predictability between post synthesis and post layout results. It is evident that synthesis and placement technologies must merge to create properly placed and routable designs that meet realistic performance goals.

WP123 **Using FPGAs with ARM Processors (v1.0) 08/18/00 (85 KB)** FPGAs

This white paper discusses interfacing Xilinx FPGAs with off-the-shelf ARM processors. It covers some of the available ARM Application Specific Standard Products (ASSPs) and describes some of the Xilinx plus ARM development systems currently available for engineers to evaluate. Techniques and features that improve design performance are also included to help achieve maximum throughput.