## White Papers by Number



- **By Number**
- By Date
- By Product


| Number | White Paper Description | Product |
|---|---|---|
| **WP100** | **Xilinx at Work in Set-Top Boxes (v1.0) 03/28/00 (150 KB)**<br>This White Paper gives an overview of different set-top box technologies and how Xilinx high volume programmable devices can be used to implement complex system level glue in a variety of set-top box designs. It concentrates on set-top box technology used to receive television over satellite, cable and terrestrial channels. | CPLDs, Spartan-II |
| **WP102** | **Xilinx at Work in Digital Printers (v1.0) 12/13/99 (91 KB)**<br>This white paper focuses on the market size for the various printer technologies, both by performance and geographic region. It then discusses the basics of the technologies, to give a view of their capabilities, limitations and future directions. It will then focus on exactly where Xilinx XC9500XL CPLDs and Spartan FPGAs play a vital role in this important market, then take a look into the future direction it is headed with Internet influence and the new photographic quality printers and MFPs. | CPLDs, Spartan FPGAs |
| **WP103** | **Xilinx High Volume Programmable Logic Applications in Internet Audio Players (v1.0) 01/17/00 (120 KB)**<br>This paper provides an overview of Internet audio technologies and how Xilinx high-volume programmable devices can be used to overcome some of the significant challenges facing the designers of portable players. The Xilinx device families targeted at these high-volume applications include CoolRunner™ CPLDs and Spartan™ FPGAs. | CPLDs, Spartan FPGAs |
| **WP105** | **CoolRunner XPLA3 CPLD Architecture Overview (v1.0) 01/06/00 (235 KB)**<br>This document describes the CoolRunner™ XPLA3 CPLD architecture. | CoolRunner XPLA3 CPLDs |
| **WP106** | **The Spartan-II Family — The Complete Package (v1.0) 01/06/00 (338 KB)**<br>The Spartan™-II Family, Combined with a Vast Soft IP Portfolio is the First Programmable Logic Solution to Effectively Penetrate the ASSP marketplace. Spartan-II offer more than 100,000 system gates at under $10 and are the most cost-effective PLD solution ever offered. They build on the capabilities of the very successful Virtex family and supports all the associated features, including SelectIO™, BlockRAM™, Distributed RAM, DLLs, and support clock speeds up to 200 MHz. Spartan-II extends the Spartan family focus in competing against ASICs and is uniquely poised to penetrate the ASSP marketplace. | Spartan-II |
| **WP107** | **Inverse Multiplexing for ATM (IMA) Solutions with Spartan-II (v1.0) 01/11/00 (87 KB)**<br>Early deployment of IMA technology meeting the IMA v1.0 standard began in late 1997 but due to different interpretations of this specification, true multi-vendor interoperability was not really possible until the completion and acceptance of the IMA v1.1 specification in 1999. With the introduction of the Spartan-II family of devices and the IMA-8 and other Xilinx based IMA core solutions, an FPGA based IMA implementation is simple and economical. | Spartan-II |

# DataSource CD-ROM Q4-10: White Papers by Number

**WP108**  **CoolRunner XPLA3 Clocking Options (v1.0) 09/13/00 (58 KB)**

This document gives a detailed description of the CoolRunner XPLA3 clocking options.

CoolRunner XPLA3 CPLDs

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**WP109**  **HDLC Controller Solutions with Spartan-II (v1.0) 02/01/00 (145 KB)**

Using the Spartan™-II Family in combination with a Soft IP to effectively penetrate the HDLC Controller market in place of the traditional ASSP.

Spartan-II

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**WP110**  **Reed-Solomon Solutions with Spartan-II (v1.0) 02/10/00 (148 KB)**

This paper explains the theory behind Reed-Solomon error correction, and discusses how a variety of practical Reed-Solomon encoding/decoding solutions can be implemented using Xilinx Spartan™-II family FPGAs.

Spartan-II

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**WP111**  **Spartan-II Family as a Memory Controller for QDR-SRAMs (v1.0) 02/16/00 (110 KB)**

The explosive growth of the Internet is boosting the demand for high-speed data communication systems. In order to increase memory bandwidth significantly for future high-performance communication applications, Cypress Semiconductor, Integrated Device Technology, Inc. and Micron Technology have jointly defined and developed a new SRAM architecture referred to as the Quad Data Rate™ (QDR™) SRAM technology. FPGAs are ideal to implement the control and interface logic, which ties the CPUs to the QDR SRAMs. The Spartan™-II FPGA, with its unique and extensive features is an ideal memory controller interface for the QDR SRAM. Spartan-II offer more than 100,000 system gates at under $10 and are the most cost-effective programmable logic devices (PLD) solution ever offered.

Spartan-II

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**WP113**  **A Spartan-II DCT/IDCT Programmable ASSP Solution (v1.0) 02/25/00 (180 KB)**

This paper presents an overview of Discrete Cosine Transform (DCT) and Inverse Discrete Cosine Transform (IDCT) solutions using XIlinx Spartan™-II components with IP core technology from Xilinx AllianceCORE™ partner Xentec, Inc.

Spartan-II

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**WP114**  **High-performance Spartan-II 8-bit Microcontroller Solution (v1.0) 03/16/00 (165 KB)**

Using the Spartan™-II Family in combination an 8-bit microcontroller Soft IP to effectively penetrate Industrial instruments and Consumer Applications. This white paper presents a brief history, the market space for 8-bit microcontrollers, the Spartan-II 8-bit microcontroller solutions, 8051 IP solutions, applications and the Spartan-II FPGA advantage.

Spartan-II

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**WP115**  **Data Encryption using DES/Triple-DES Functionality in Spartan-II (v1.0) 03/09/00 (332 KB)**

Today's connected society requires secure data encryption devices to preserve data privacy and authentication in critical applications. There is an immense value in integrating critical IP solutions like Discrete Cosine Transform/Inverse DCT (DCT/IDCT) and DES within a Xilinx Spartan-II FPGA to enhance performance and security in communication applications.

Spartan-II

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**WP116**  **Xilinx Spartan-II FIR Filter Solutions (v1.0) 04/05/00 (317 KB)**

Traditionally, digital signal processing (DSP) algorithms are implemented using general-purpose programmable DSP chips for low-rate applications. Alternatively, special-purpose, fixed function DSP chipsets and application-specific integrated circuits (ASICs) are used for high-performance applications.

Spartan-II

**WP118** **Using CoolRunner CPLDs in Smart Card Reader Applications (v1.0) 05/18/00 (222 KB)**

CoolRunner XPLA3 CPLDs

This document presents the different types of smart cards and their applications and discusses the variety of smart card readers available and what functions they can perform. An illustration of the elements that form a typical smart card reader and how and where CoolRunner devices can be used to undertake some of these tasks is described herein.

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**WP119** **Fast Zero Power (FZP™) Technology (v1.0) 08/28/00 (52 KB)**

CoolRunner XPLA3 CPLDs

This white paper provides an overview of the patented Fast Zero Power (FZP™) technology used in Xilinx CoolRunner CPLDs.

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**WP120** **Xilinx High-Volume Programmable Logic Applications in Satellite Modem Designs (v1.0) 073/21/00 (74 KB)**

CPLDs Spartan FPGAs

This paper provides an overview of satellite modem technologies and standards, and discusses how the Internet is driving the deployment of this technology. The Xilinx device families targeted at these high volume applications include XC9500 CPLDs and Spartan &#reg; -II FPGAs.

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**WP122** **Using the CoolRunner XPLA3 Timing Model (v1.0) 09/13/00 (103 KB)**

CoolRunner XPLA3 CPLDs

This document describes how to use the CoolRunner &#reg; XPLA3 timing model.

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**WP123** **Using FPGAs with ARM Processors (v1.0) 08/18/00 (85 KB)**

FPGAs

This white paper discusses interfacing Xilinx FPGAs with off-the-shelf ARM processors. It covers some of the available ARM Application Specific Standard Products (ASSPs) and describes some of the Xilinx plus ARM development systems currently available for engineers to evaluate. Techniques and features that improve design performance are also included to help achieve maximum throughput.

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**WP124** **Xilinx at Work in Digital Modems (v1.0) 5/19/99**

CPLDs, Spartan FPGAs

This white paper gives an overview of digital modem technologies and how Xilinx high volume programmable devices can be used to implement complex system level glue in digital modem designs.

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**WP125** **Xilinx at Work in ISDN Modems (v1.0) 5/19/99**

CPLDs, Spartan FPGAs

This white paper gives an overview of ISDN modem technologies and how Xilinx high volume programmable devices can be used to implement complex system level glue in ISDN modem designs.

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**WP128** **Introduction to Home Networking (v1.0) 03/21/01 (453 KB)**

Spartan-II

Once connected, consumers find innumerable uses for their home networks. Home networking is really a three part equation offering entertainment, information, and automation services that are distributed between appliances in the home.

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**WP129** **Introducing Xilinx and Programmable Logic Solutions for Home Networking (v1.0) 03/21/01 (870 KB)**

Spartan-II

dynamics in these markets. The eSP: Home Networking program helps system designers and ASIC/FPGA designers understand the technology and market dynamics to make the right decisions in this marketplace.

**WP130** **Broadband Access (v1.0) 03/21/01 (510 KB)** Spartan-II

The Internet continues to expand at an enormous rate, and the worldwide modem market will continue to be buoyed by this growth as the default solution for residential Internet access. Cable and xDSL modems will continue their strong movement into the residential marketplace. Today, applications such as Internet access and high-speed remote access to storage media require more data capacity than traditional telecommunications services can provide. Replacing copper wiring with fiber optic cabling is one way of delivering this capacity to your home, but the associated technology is expensive.

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**WP131** **Media (Residential) Gateways (v1.0) 03/21/01 (654 KB)** Spartan-II

The primary function of the media gateway is to provide broadband connectivity to the home through cable, xDSL, satellite, and wireless. Secondly, media gateways will provide home networking capabilities by distributing broadband access throughout the home using technologies such as HomePNA (phonelines) or wireless LANs. The demand for greater Internet bandwidth is driving the need for digital modem solutions. This white paper looks at utilizing an existing PC to provide media gateway type services. Companies like IBM and Ericsson are strongly promoting this concept.

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**WP132** **Information (Internet) Appliances2 (v1.0) 03/21/01 (440 KB)** Spartan-II

Market researchers predict that information appliances will out-ship consumer PCs by 2002 in the U.S. High-volume information appliances will be products such as digital TV, DVD players, digital cameras, and handheld devices. Semiconductors enable new devices and players, but technology is increasingly becoming invisible. Xilinx programmable logic products (Spartan™-II FPGAs, CoolRunner™, and 9500 CPLDs) ported with intellectual property (IP) provide solutions like ASSPs, but with increased flexibility. FPGA logic not used from the IP can be programmed with other IP cores—such as embedded solutions. Other features within the Spartan-II provide system integration, and the reprogrammability enables time-to-market and flexibility at low costs. Xilinx Online™ allows time-in-market as specifications in emerging technologies keep evolving.

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**WP133** **Home Networking Using “No New Wires“ Phoneline and Powerline Interconnection Technologies (v1.0) 03/21/01 (357 KB)** Spartan-II

In the context of a home networking environment, “no new wires“ is the term applied to a suite of technologies that use existing wiring systems to distribute high-speed data and video throughout your house. Phoneline and powerline systems are the two dominant “no new wires“ technologies.

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**WP134** **Home Networking Using “New Wires“ — IEEE 1394, USB, and Fast Ethernet Technologies (v1.0) 03/21/01 (546 KB)** Spartan-II

With the proliferation of digital television more and more people around the world are beginning to distribute audio and video signals around their homes. For the home networking purists, Ethernet equipment offers inexpensive and proven products that can be bought at retail in both kit form or a la carte. Ethernet technology can reliably and efficiently network all the Internet appliances (PCs, printers, game consoles, digital televisions, security cameras, and much more) at home. Xilinx solutions enable these evolving technologies in consumer devices today.

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**WP135** **Wireless Home Networks — DECT, Bluetooth, HomeRF, and Wireless LANs (v1.0) 03/218/01 (537 KB)** Spartan-II

A wireless home network is an intriguing alternative to phoneline and powerline wiring systems. Wireless home networks provide all the functionality of wireline networks without the physical constraints of the wire itself. They generally revolve around either IR or radio transmissions within your home. Radio transmissions comprise of two distinct technologies—narrowband and spread-spectrum radio. Most wireless home networking products are based upon the spread-spectrum technologies. To date, the high cost and impracticality of adding new wires have inhibited the wide spread adoption of home networking technologies. Wired technologies also do not allow users to roam about with portable devices. In addition, multiple, incompatible communication standards have limited acceptance of wireless networks in the home.

**WP136**  **Home Networking Middleware (v1.0) 03/21/01 (881 KB)** Spartan-II

This white paper presents an overview of how home networking middleware supports the seamless convergence of broadcast and home network applications. The fusion between both of these technologies facilitates the deployment of a range of new entertainment services within the home. UPnP leverages Internet and Web components (like IP, TCP, UDP, HTTP, and XML) and enables seamless proximity networking in addition to control and data transfer among networked appliances in the home, office, and everywhere else.

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**WP137**  **Intellectual Property (IP) Cores for Home Networking (v1.0) 03/21/01 (81 KB)** Spartan-II

Spartan™-II FPGAs, programmed with IP cores, enable home networking products. Xilinx develops IP cores and partners with third-party IP providers to provide customers with a suite of cores to decrease the customer's time-to-market. W While reprogrammability reduces the customer's time-to-market and enables flexibility, the Xilinx Online™ program allows time-in-market as specifications in emerging technologies keep evolving.

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**WP138**  **Voice-Data Convergence—Voice Over IP (v1.0) 03/21/01 (359 KB)** Spartan-II

This paper gives an overview of voice-data convergence technologies and how Xilinx high volume programmable devices can be used to overcome some of the significant challenges facing the designers of these systems. The Xilinx products targeted at these high-volume applications include XC9500XL™ and CoolRunner™ CPLDs and Spartan™-II FPGAs. This appendix starts with an overview of voice-data convergence technologies and the benefits they bring to the users. We will then describe the product architectures that are used to implement VoIP gateways and IP phones. The final topic will be to show how Spartan-II devices can be used in these applications.

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**WP139**  **FPGA Enabled Home Networking Technology Bridges—Connecting Disparate Technologies (v1.0) 03/21/01 (118 KB)** Spartan-II

The digital age of consumer electronics is here and it is bringing with it faster computing at lower costs. The Internet revolution and distribution of broadband access to different digital consumer electronics and their interoperation introduces a new wave of technology into your home. Home networking involves distribution of audio, video, and data around the home and ensures interoperability between various information appliances in your home. Home networking has four aspects, which include broadband access, residential gateways, a vast range of information appliances, and the technologies that bind them all—interconnectivity or home networking technologies.

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**WP140**  **Physical Synthesis (v1.0) 02/26/01 (32 KB)** Spartan-II

In the domain of deep submicron (DSM) and nanometer ASIC technologies (180 nm and below), the traditional separation between logical (synthesis) and physical (place and route) design methods often causes a problem—designs cannot meet their realistic timing objectives; creating the well known “timing closure problem.“ Timing closure is now considered the biggest area of difficulty for ASIC performance-oriented designs. The underlying reason is that circuit delays are dominated by net delays, which are influenced by the placement of the cells. The traditional fanout-based wireload models, for estimating interconnect delay during synthesis, are considered inaccurate and are the key factor causing the lack of timing predictability between post synthesis and post layout results. It is evident that synthesis and placement technologies must merge to create properly placed and routable designs that meet realistic performance goals.

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**WP141**  **UART to PCMCIA Bridging for Bluetooth (v1.0) 04/27/01 (433 KB)** Spartan-II

A Xilinx based fast UART to PC Card (PCMCIA) bridging solution is the ideal mechanism for integrating industry standard Bluetooth communications into legacy systems. Such a solution can be realized quickly, can leverage a wide variety of low cost Bluetooth components, and can be optimized to impose a minimal impact on the host system implementation and performance. The result is a cost effective solution, fast time-to-market, and preservation of host MIPS for the primary device application.

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**WP142**  **UART to PCI Bridging for Bluetooth Applications (v1.0) 04/27/01 (188 KB)** — Spartan-II

A Xilinx UART (Universal Asynchronous Receiver and Transmitter) to PCI (Peripheral Component Interconnect bus) bridging solution is ideal to integrate the emerging Bluetooth communications standard into legacy systems. It leverages a wide variety of low-cost Bluetooth components, and can be quickly implemented and optimized to ensure minimal impact on host system performance. The result is a fast-to-market, cost effective solution that preserves host MIPS for the primary device application.

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**WP143**  **Xilinx Generic Flash Memory Interface Solutions (v1.0) 05/08/01 (186 KB)** — Spartan-II

This white paper shows how a generic flash memory interface can be combined with Xilinx IP interface cores to add flash memory to Xilinx Spartan device designs.

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**WP145**  **UART to Powerline Bridging for Bluetooth (v1.0) 05/08/01 (107 KB)** — Spartan-II

This white paper shows how a generic flash memory interface can be combined with Xilinx IP interface cores to add flash memory to Xilinx Spartan device designs.

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**WP146**  **UART to 1394 Bridging for Bluetooth (v1.0) 05/08/01 (208 KB)** — Spartan-II

The distribution of video, audio, and PC data has evolved using a variety of different networking technologies. Various factors drive these applications including cost, performance, quality of service required, regulatory issues, geographic building trends, etc. Therefore, Ethernet, IEEE 1394, Bluetooth, USB, HomePNA, HomePlug, HomeRF, HiperLAN2, and Wireless LAN are available to network homes and/or small offices. Each one of these technologies has its own pros and cons and is suitable for specific applications.

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**WP148**  **The ABC's of 2.4 and 5 GHz Wireless LANs (v1.0) 08/01/01 (2.3 MB)** — Spartan-II

The enterprise, SOHOs, and homes are demanding mobility and portability with high-bandwidth data, voice, and video access. This has led to the introduction of wireless LAN technologies, which attempt to provide exactly that. In the 2.4 GHz frequency band, IEEE 802.11b is “the“ wireless LAN solution in the market. However the 5 GHz frequency has two possible contending technologies — IEEE 802.11a and HiperLAN2. This white paper explains the state of affairs in the wireless LAN market, the underlying technology behind the different types of wireless LANs, the over-utilized 2.4 GHz spectrum, the migration to 5 GHz band, which technology will succeed, and how Xilinx Spartan-II are ideal for this market place.

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**WP150**  **Solving the Challenges for Terabit Networking and Beyond (v1.0) 07/20/01 (114 KB)** — Global Services

In today's world of modular networking and telecommunications design, it is becoming increasingly difficult to keep alignment with the many different and often changing interfaces, both inter-board and intra-board. Each manufacturer has their own spin on the way in which devices are connected. To satisfy the needs of our customers, we must be able to support all their interface requirements. For us to be able to make products for many customers, we must adopt a modular approach to the design. This modularity is the one issue that drives the major problem of shifting our bits from one modular interface to another.

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**WP151**   **System Ace: Configuration Solution for Xilinx FPGAs (v1.0) 09/25/01 (58 KB)** — Configuration Solutions

Design techniques for electronic systems are constantly changing. In industries at the heart of the digital revolution — telecommunications, networking, and wireless communications — this change is especially acute. Functional integration, dramatic increases in complexity, new standards and protocols, and increased time-to-market pressures have bolstered both the design challenges and the opportunities in architecting modern electronic “boxes.” One trend driving these changes is the increased integration of core logic with previously discrete functions to achieve higher performance and more compact board designs. Traditionally, ASICs have been the vehicle for such integration but now, with their advanced system capabilities, programmable logic devices (PLDs), especially field programmable gate arrays (FPGAs), have begun to take on this role in system design.

**WP152** NEW!

**Xilinx FPGA Configuration Data Compression and Decompression (v1.0) 09/25/01 (32 KB)**

Configuration Solutions

This document provides a brief description of the Xilinx bitstream compression algorithm based on the LZ77 scheme. FPGA configuration files can be compressed by Xilinx-developed software to reduce memory storage requirements. Compressed configuration files can be stored in a high-density System ACE™ MPM FPGA configuration controller. The System ACE MPM controller decompresses the files and shifts the original configuration data to the target FPGAs.