WP137 (v1.0) March 21, 2001

Intellectual Property (IP) Cores for Home Networking

Author: Amit Dhir

Summary

Spartan™-II FPGAs, programmed with IP cores, enable home networking products. Xilinx develops IP cores and partners with third-party IP providers to provide customers with a suite of cores to decrease the customer's time-to-market. While the FPGA plus IP core solution provides functionality and performance similar to ASSPs, they also provide an unparalleled flexibility. With increased densities, Spartan-II FPGAs provide embedded solutions—where the FPGA logic not used from IP can be programmed with other IP cores. Also, other features such as clock management, system I/O capabilities, and embedded memory provide system integration. This combined with the effective costs increases the value proposition of Spartan-II FPGAs, while reducing the overall solution cost.

While reprogrammability reduces the customer's time-to-market and enables flexibility, the Xilinx Online™ program allows time-in-market as specifications in emerging technologies keep evolving.

Introduction

Today, a large number of predefined cores are available to implement system-level functions directly in Xilinx PLDs. These cores, available from Xilinx and third-party partners, allow designers to cut design time and significantly reduce risk while having access to the best performing and lowest cost components available. Full information about Xilinx cores is available on-line from the IP Center area of the Xilinx website. Visit the IP center at:

www.xilinx.com/ipcenter

LogiCORE™ products are sold and supported directly by Xilinx and include IP cores such as system interfaces such as PCI, digital signal processing (DSP) functions, and a number of other modules such as adders, multipliers, and look-up tables. These IP cores are optimized for Xilinx FPGAs and CPLDs to provide the highest performance while taking the lowest area.

AllianceCORE™ modules are sold and supported by a network of third-party developers and are optimized for Xilinx devices. This program has allowed Xilinx to expand the availability of high-quality cores for PLDs through a cooperative effort between Xilinx and independent third-party cores developers. Current AllianceCORE products range from processors and standard peripheral controllers to ATM functions. Xilinx works closely with its partners in the process of cataloging AllianceCORE products to raise the quality and usability of the cores that are offered. A core must meet a minimum set of criteria before it can receive the AllianceCORE label.

Smart-IP Core Design Methodology

Smart-IP™ technology is a combination of several features designed to deliver highest performance, predictability, and flexibility when implementing IP with Xilinx FPGAs. Smart-IP technology ensures constant core performance regardless of its position in the FPGA device; maintained performance when multiple cores are integrated in the same FPGA device; and no performance degradation when migrating to larger devices. The IP is built so that it makes use of the unique features of the Spartan-II architecture such as dedicated multiplier or multiplexor logic. The use of Smart-IP technology means that the performance of the core is independent of core placement, number of cores used, surrounding user logic, device size, and EDA tools.

The CORE Generator™ tool from Xilinx delivers highly optimized cores that are compatible with standard design methodologies for Xilinx FPGAs. This easy-to-use tool generates flexible, high-performance cores with a high degree of predictability and allows customers to download future core offerings from the Xilinx website. Both Xilinx and independent IP developers can

design cores for the CORE Generator tool, which also serves as a cataloging and delivery system for related collateral for all designers using Xilinx.

CORE Generator features:

- Simple, intuitive operation: Select a core, enter parameters, and generate
- Compatible with VHDL, Verilog, and schematic top-level design flows
- Cores are delivered with a logic design plus an optimal floorplan or layout
- Performance is independent of FPGA device size
- Performance stays constant as more cores are added
- Optimal results as measured against the best hand-packed design
- Data sheet and VHDL behavioral model with each core
- Ready access to intellectual property from Xilinx and Xilinx partners
- Predictable and repeatable results: core performance is specified in advance
- PC and Workstation platforms supported

CORE Generator benefits:

- Faster time-to-market
- Fast core generation time with proprietary Xilinx software
- Reduced place and route time with preplaced cores
- Less engineering required with predesigned cores
- Facilitates design reuse
- Build your design out of cores
- Simpler documentation with larger parameterizable building blocks
- Optimal core layout produces lower power dissipation

Spartan-II IP Support

The Spartan-II family has had very robust core support since the time of its introduction. Xilinx has a range of IP cores such as memory controllers, system interfaces, DSP, communications, networking, and microprocessors.

The extensive IP library today includes the following cores:

- **BaseBlox**: UARTs, multipliers, DMA
- **Memory/Memory controllers:** Embedded memory, SRAM controllers, SDRAM controllers
- **Networking and communications**: Cell assembler, cell delineation, CRC, T1 Framer, HDLC controllers, 10/100 Fast Ethernet, UTOPIA, ATM/IP over SONET, ADPCM, IMA, SONET, OC-48, OC-192, VoIP, Reed-Solomon FEC, Viterbi FEC, xDSL modems, cable modems, satellite modems, UMTS, W-CDMA
- **Microcontrollers, microprocessors:** 8051, 8-bit, 32-bit RISC processors
- **DSP:** FIR filters, comb filters, FFT, color space converter, DCT/IDCT video and image processing, DES, triple DES, MP3, QAM, QPSK, JPEG, speech recognition, programmable DSP engines
- **System I/O, standard bus interfaces**: Two-wire serial interface, CAN (Car Area Network), ISA, I2C, PCI (32- and 64-bit, 33 and 66 MHz), Compact PCI Hot-Swap, PC-104, VME, AGP, USB/USB2.0, IEEE-1394/FireWire, PCI-X 133 MHz and other emerging high-speed standard interfaces

This extensive IP library allows the Spartan-II FPGAs to compete against ASSPs. With the high densities, extensive features, low cost, and flexibility of the Spartan-II FPGAs, they can effectively penetrate the ASSP market.

IP for Home Networking

I/O Control and System Interface

Set-top boxes, residential gateways, and SOHO routers have multiple front-end and multiple back-end technologies to support. Front-end technologies provide broadband (digital or analog) interface from the cable companies, telcos, and satellite service providers using xDSL, cable, satellite, wireless, powerline, or analog phone dial-up. With consumer products increasingly becoming networked, the home gateway requires the capability to network multiple islands of technologies. These home networking technologies may use existing wires (phonelines, powerlines), new wires (Ethernet, FireWire/IEEE 1394, Fiber Optic, USB/USB 2.0) and wireless (HomeRF, Bluetooth, and wireless LANs—IEEE 802.11a, IEEE 802.11b, HiperLAN2).

Success of products is based not only on the pros and cons of the home networking and consumer markets but also on the geography. While DSL may be the broadband access of choice in a location, cable may be the technology of choice at another. It is not cost effective for manufacturers to support multiple receivers and build individual products for cable, terrestrial, xDSL, and satellite. Slicing the market and building multiple gateway designs based on different home networking technologies is resource and cost prohibitive. This approach also prevents OEMs from second-guessing if other technologies will prevail, and if their products will succeed in the market.

Spartan-II FPGAs provide the interface required to support multiple receiver and multiple home networking ASSPs. This provides a low-cost protocol translation mechanism between two disparate technologies and an interface to the system.

In addition, the ASSP used is influenced not by the gateway manufacturer but by broadcaster features, hence making it near to impossible for the set-top box or gateway manufacturer to bring a product to market soon.

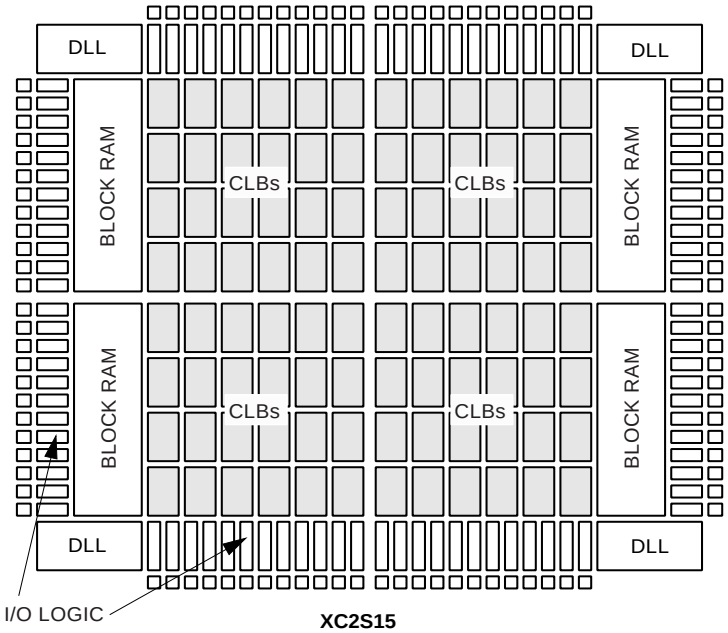

Figure 1: **Architecture on Spartan-II FPGAs**

Hard Disk Drive (HDD) Interface

New digital VCRs, set-top boxes, and residential gateways provide the capability to store audio and video on HDDs. They also provide the ability to record and view video simultaneously. Spartan-II FPGAs provide HDD interfaces in these products.

These devices provide data buffer and disk control logic with on-chip memory for FIFOs. Programmable solutions allow support of evolving disk drive technologies, and are optimized

for simultaneous disk read and write. Also, with millions of set-top boxes being shipped per year Spartan-II devices enable dual sourcing of multiple types of HDDs in case of a supply shortage.

Spartan-II FPGAs truly help revolutionize the TV experience by being at the heart of evolving set-top boxes. The ability to pause live TV, instant replay, automatically record favorite programs, and perform advanced TV program search is truly revolutionary.

Delay-Locked Loop (DLL) Technology

Spartan-II includes powerful chip and board level clock management with DLL technology. DLL is the digital implementation of the analog phase-lock loops (PLLs). Spartan-II includes four DLLs in each device. Each DLL is capable of removing on-chip and board level clock delays. This allows you to get clock-to-out times of less than 3.5 ns on even the largest Spartan-II device.

Using these clock management functions can save cost in the system by allowing slower speed clocks on the board (which are then multiplied by the DLL internally) or through the use of slower access time memories (since the internal clock delays are reduced and chip performance improved). This allows lower memory and board costs.

- The DLL circuits in Spartan-II FPGAs provide full clock management solution, which includes:
- **Clock generation:** synthesizing many clocks from a single reference crystal or clock.
- **Clock buffering and distribution:** provides multiple copies of a single clock
- **EMI reduction:** DLL circuits allow tolerance for ±2.5 percent variance which is ideal for spread spectrum clocks

Memory Solutions

Spartan-II FPGAs have distributed RAM and block RAM used for FIFOs and buffers. They are also used as memory controllers to interface with the different types of memories such as SRAM, SDRAM, and flash. With the increased density in the Spartan-II family, we have also improved the memory offerings and thus enabled many new applications.

The Spartan and Spartan-XL families only had the look-up table based distributed RAM elements. These are excellent for small storage elements such as are found in DSP processing or small FIFOs. The Spartan-II family retains the distributed RAM and adds the larger block RAM elements. These are excellent for large FIFOs and buffers such as video line buffers or packet buffers in small office routing equipment.

In addition to these two forms of internal memory, the high-bandwidth I/Os in the Spartan-II family can operate with external memory and other ASSPs at the same high 200 MHz rate as the internal memory accesses. This transparent bandwidth across internal and external memory allows the system designer maximum flexibility so that the system can be architected for maximum cost savings.

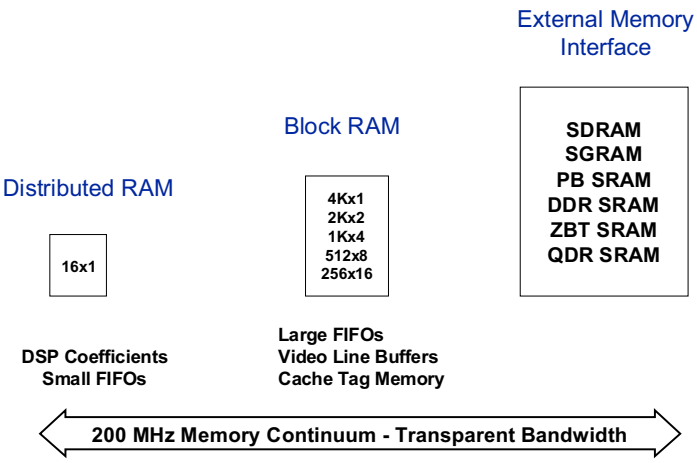

Figure 2: **Embedded Memory Solutions from Xilinx Allow 200 MHz Memory Continuum Between Internal and External Memories**

The Spartan-II block RAM elements are very flexible and competitive. They are 4K bits per block and are a true dual port design, and can be read and written on each port individually. The widths of the two ports are individually configurable from 1 to 16 bits wide. These RAM blocks are very fast with a 2.5 ns clock-to-output time and 1 ns of address setup.

The Spartan-II FPGA, with its unique and extensive features, provides a flexible architecture to be a memory controller for interface with different types of SRAM, DRAM, and flash. Moreover, Xilinx provides FREE VHDL source code (reference designs) for implementing the memory controllers in the low cost Spartan-II FPGA.

Xilinx introduced a comprehensive website detailing memory and the different solutions available. It was a collaboration effort between Xilinx and major memory vendors to provide comprehensive web-based memory solutions. This website is educational to include data sheets, application notes, tutorials, FAQs, design guidelines, and white papers. It also provides free reference designs (VHDL/Verilog) for SRAM, DRAM, and embedded FPGA memory solutions, thus making it a one-stop-shop for all your memory requirements. More information on this can be obtained from:

http://www.xilinx.com/products/xaw/memory/

Peripheral Component Interconnect (PCI) Solutions

PCI has become one of the most popular bus standards, not only for personal computers, but also for industrial computers, communication switches, routers, and instrumentation. It solves a wide range of compatibility problems and performance limitations that were encountered with the older ISA and VME standards.

However, PCI is also a significant design challenge; the stringent electrical, functional, and timing specifications are difficult to meet in any technology—and the standard keeps evolving to meet the dynamic needs of our industry. That's why you need a flexible PCI solution that will meet both your current and future requirements, while guaranteeing full PCI compliance with no limitations on performance or functionality.

The first LogiCORE PCI product was released in January 1996. Now, PCI cores have been proven in over 1,000 customer designs, clearly demonstrating that RealPCI™ from Xilinx is the most flexible and cost-effective solution for your fully-compliant, high-performance PCI system. Visit the Xilinx IP center for more details and data sheets on individual products:

http://www.xilinx.com/ipcenter

Xilinx DSP Solutions

With Xilinx DSP, users can combine ASIC-like performance and integration with the flexibility of a DSP processor implementation. By using parallel computing techniques in a Xilinx FPGA, users can achieve radical performance advantage over fixed processors. The Xilinx FPGA implementation will, at the same time, maintain maximum flexibility and the shortest time-to-market, which is lost using an ASIC implementation. Until now, tools to automate the design process have been lacking and only experienced FPGA designers have completed most designs manually. With the introduction of the Xilinx CORE Generator System for DSP, complex parameterized DSP building blocks can be implemented automatically with the performance and density of a hand-tuned implementation. LogiCORE DSP modules can be used with VHDL-, Verilog-, or schematic-based design methodologies.

Xilinx recently announced XtremeDSP™ solutions which deliver the performance and flexibility needed to build complex, high-performance DSP solutions such as 3G and 4G wireless communications, high-speed networking, real-time video broadcasting, and high-performance computing systems.

AllianceCORE Program

Through the AllianceCORE program, Xilinx is expanding the availability of high-quality cores for programmable logic by sharing what has been learned with leading third-party core developers. The AllianceCORE program is a cooperative effort between Xilinx and independent third-party IP core developers. It is designed to produce a broad selection of industry-standard solutions dedicated for use in Xilinx programmable logic. Xilinx takes an active role with its partners in the process of cataloging AllianceCORE products and works closely with partners to select the right cores first which helps raise the quality and usability of the cores that are offered. Some of Xilinx AllianceCORE IP products qualified for Spartan-II FPGAs are:

- MPEG decoder
- 10/100 Ethernet MAC
- IEEE 1394 Link Layer core
- T1 Framer
- CAN (car area network) bus interface
- Forward error correction: Reed-Solomon, Viterbi, Convolutional
- Conditional access and encryption: DES, triple DES, proprietary
- CPU/microcontroller: 8-bit, 8051, 32-bit RISC
- HDLC (high-level data link control) controller
- ADPCM (adaptive differential pulse code modulation) codec
- DVB satellite modulator
- Color space converters
- DCT/IDCT (discrete cosine transform/inverse DCT) imaging solutions
- JPEG codec
- Glue logic for system integration: LCD controllers, UARTs, DMA controllers

For more details, data sheets and other information on LogiCORE and AllianceCORE products, please visit the Xilinx IP center website:

http://www.xilinx.com/ipcenter

Increased densities allow the Spartan-II family to be programmed with IP cores and provide the functionality and performance similar to ASSPs. Spartan-II FPGAs through its infinite programmability capabilities provide the flexibility needed in dynamic evolving markets. With spare FPGA gates, the Spartan-II devices can be programmed with other IP blocks or other glue logic. For example, programming a single Spartan-II FPGA with DCT/IDCT and DES/TDES soft IP provides multimedia, imaging, and encryption applications.

The Spartan-II family moves the FPGA from glue logic to system level component by addressing more than the logic needs of the designer. It helps the designer solve board level challenges previously left to the designers to solve with external components. Spartan-II features such as memory, translators, and DLL circuits help provide additional savings.

Spartan-II FPGAs are the perfect programmable system integration vehicle, providing high-bandwidth communication interface to external devices such as ASSPs, CPUs, memory, and backplane. This eliminates the need for custom logic, expensive clock management schemes, and various translator components including direct interface to backplanes with its system I/O capabilities. Integration of these simple ASSP functions (PLLs, FIFOs, level translators, etc.) can save the user considerable cost.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/21/01	1.0	Initial Xilinx release.