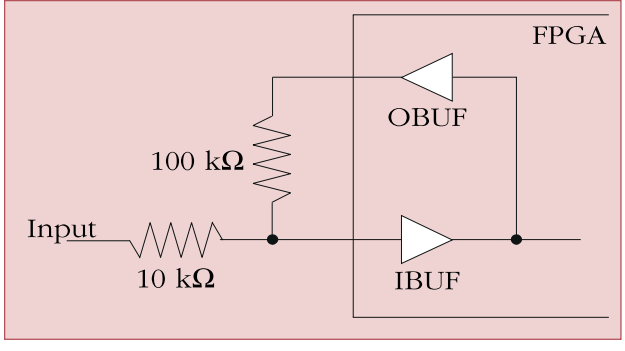
User-Defined Schmitt Triggers

All inputs to Xilinx FPGAs have a hysteresis of 100 to 200 mV. It helps avoid noise propagation from slowly rising or falling input signals. Users requiring more hysteresis can design their own **Schmitt trigger** circuits easily with only two resistors. However, it uses one additional output pin, driven (non-inverted) from the input pin, as in the diagram.

A 10 kΩ serial input resistor combined with a 100 kΩ feedback resistor gives 500 mV of hysteresis. (Hysteresis is the difference between the effective input threshold voltages on the Low-to-High transition and the High-to-Low transition. That difference is equal to V_{CC} times the resistor ratio.)



A 1 kΩ/10 kΩ combination gives the same hysteresis, but reduces the delay caused by the pin-to-ground capacitance from 100 ns to 10 ns. On the other hand, it requires more input current.

For TTL-threshold inputs, the hysteresis should be kept below 1 V; for CMOS inputs, it can be up to 2 V. ◆