FPGAs Control ATM Connections to French Telecom Network

The Lannion-based laboratory of France Telecom's research center, **Centre National d'Etudes des Telecommunications** (CNET), has found Xilinx FPGAs useful in its research on Asynchronous Transfer Mode (ATM) telecommunications for high-speed communications over ordinary telephone lines. One of seven laboratories operated by France's public telephone company, CNET engineers have been designing, building and testing prototypes of the equipment needed to allow a public network operator to offer ATM connections.

One such piece of equipment, dubbed the "Spacer-Controller," is part of the interface between the sources of the ATM streams and the public ATM network. The Spacer-Controller must check that each received cell conforms to the traffic parameters allowed on that substream. This policing function is referred to as Usage Parameter Control (at the User Network Interface) or Network Parameter Control (at the Broadband Inter Carrier Interface) in the International Telecommunications Union (ITU) standards. This check is performed using an ITU standard algorithm developed at CNET called the "Virtual Scheduling Algorithm." Subsequent to this check, a spacing function ensures the the timely smoothing out of cells belonging to the same substream in accordance with a predefined Peak Emission Interval.

Based on eight years of experience with the high integration levels and ease-of-use of Xilinx FPGAs, the CNET engineers chose members of the XC3100 family for fast prototyping of these highly complex ATM traffic functions

Driven by a 20 MHz clock, four XC3190 FPGAs implement the policing and spacing functions. At the heart of these functions are the multiple 32-bit adders and comparators used for the Virtual Scheduling Algorithms. A fifth XC3190 FPGA selects one of four incoming channels — two proprietary 8-bit parallel channels, one 34 Mbit/s PDH channel (Plesiochronous Digital Hierarchy, the European equivalent to T3), and one 155 Mbit/s SDH channel (Synchronous Digital Hierarchy, the European equivalent to STS-3). An XC4010 and XC4003 FPGA hold the logic for adaptation from the PDH channel to ATM format. This prototype version of the Spacer-Controller is capable of handling 4,096 VP or 65,536 ATM connections on a single link of up to 155.52 Mbit/s on a PC board.

Along with the XACT software, the CNET researchers used Viewlogic tools on a PC and Cadence tools on Sun and IBM workstations to complete the FPGA designs. Logic block utilization of the FPGAs exceeded 90 percent in all but one of the XC3190s. Completion of all the FPGA designs required an estimated one man-year of effort. A refined version currently in development will use a single high-density XC4000 series device to replace the four XC3190s that implement the policing and spacing functions.

This equipment will allow a public network operator to offer ATM connections at an attractively low cost (since the user is granted the lowest possible bandwidth allocation compatible with the application) and with as few constraints as possible (the capability for cell delay variation absorption means that the user does not need to consider the detailed traffic characteristics of his connections at subscription time). ◆

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