The Hewlett-Packard Companion Scanner - A Partnership Success Story

The Hewlett-Packard Companion scanner is a copier accessory that allows any picture or document to be scanned to an HP Laserjet printer without first downloading the data to a PC. Facing very tight time constraints, the Design Group at the HP Printer Division in Boise, Idaho realized it could not rely on fully customized ASICs as it had in the past.

According to the group's leader, Doug Keithly, they decided to use FPGAs so they could meet the planned product release date.

The FPGA vendor decision was based on three major factors:

1. Level of service (the group was new to FPGA design).
2. A proven cost-reduction path to an ASIC device.
3. The ability to support a non-VHDL PC environment (the designers did not want to spend an additional two weeks learning the rudiments of VHDL design).

HP chose Xilinx because it offered a complete HardWire ASIC cost-reduction plan (including a schedule that met their target), a schematic-based PC development environment, and on-site engineering help.

HP picked the full sea-of-gates HardWire approach for the smallest, most cost-effective die, and Xilinx provided all the vector generation and guaranteed the functionality of the ASIC.

Doug and his team began the development project with a block diagram of the system. Within a month, by using the FPGA, they had a PC board with the first implementation. By the end of the second month, they had achieved 95% functionality and were close to a final solution. During this phase, the system itself was still being defined. After the design itself was finalized, they needed two additional months for other mechanical design including paper handling, motor control, and firmware testing. Because they were constantly making changes during this phase, device programmability was key.

The HP design team used the FPGA to enhance system functionality by using the device for DSP functions, processing pixels at up to 2mb per second. Even the on-board microprocessor could not handle the data speeds required, so all of the signal processing is done by the HardWire ASIC, with the microprocessor providing set-up and coordination between functions.

After four months, HP was ready for final release. They sent the FPGA to Xilinx, and waited two weeks to receive the design conversion report, which looked clean. Within three weeks, Doug had ASIC prototypes in hand.

On the first functional test, the team discovered a potential speed problem. However, with the help of Kiran Buch, a Xilinx HardWire design expert, Doug identified an asynchronous path where speed caused a race condition. The path was not used at all in the design and Doug never checked it in the original FPGA design, so he had not applied constraints to the path as he had to all the other asynchronous paths.

Kiran sent two HP devices back to be de-capped. Using focused ion beam technology, he disabled the path and sent the parts back to Doug. The modified devices worked perfectly. Xilinx made a quick change to the mask and fabricated the modified ASIC. With the HardWire ASIC on the board, the system went to final test where the remaining system bugs were worked out.

The scanner is now in full production and Doug said, "This was a slam dunk for Xilinx. We were *really* pleased." ◆

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