Timing

Timing Analyzer will not open large report files. How can I use this tool to view large reports?

The Alliance Series 1.4 release resolves the problem on Windows NT and Workstation platforms by allowing report sizes of up to 32MB. However, Windows 95 will still continue to have this problem until an upcoming release. You may still view the large reports created by Timing Analyzer in Windows 95 by going to the directory referenced in your **TEMP** environment variable (usually **C:\WINDOWS\TEMP**) and opening the most recently modified non-empty file (prefixed by "xil_") in a text editor.

Another option is to save the report file directly to disk without relying on Timing Analyzer to display it. To do this, select **View > Console** in Timing Analyzer. In the console window that pops up, enter the equivalent command in the command field. For example, to do an **All Paths** type report, enter **AnalyzeAllPaths s c:\mydir\allpaths.twr**. Timing Analyzer will not attempt to display the file, but will save it directly to disk. The other reporting commands are **AnalyzeTimingConstraints** and **AnalyzeDesignPerformance**.

You may abbreviate these with "aap", "atc", and "adp" respectively (example: atc s c:\mydir\timing_constraints.twr).

My timing report will not show PAD to IFD or OFD to PAD paths. How can I get these timing numbers?

Currently, Timing Analyzer (or TRACE) will not report on a path from a pad to a IOB input flip-flop. This problem will be fixed in an upcoming release. It will report on the path from an IOB output flip-flop to a pad if you use the **OFFSET** constraint; however, the delay value reported may be more conservative than the "Guaranteed Input and Output Parameters" reported in the 1998 Xilinx Data Book. The pad-to-input-register and output-register-to-pad delays are fixed, so the data book's "Guaranteed Input and Output Parameters" numbers can be used.

Useful WebLINX Links to our Expert Journals

Implementation tools	http://www.xilinx.com/support/techsup/journals/implmnt/index.htm
Timing & Constraints	http://www.xilinx.com/support/techsup/journals/timing/index.htm
Foundation	http://www.xilinx.com/support/techsup/journals/foundatn/index.htm
Viewlogic	http://www.xilinx.com/support/techsup/journals/viewlogc/index.htm
Synopsys FPGA Compiler	http://www.xilinx.com/support/techsup/journals/synopsys/index.htm
Synopsys FPGA Express Users	http://www.xilinx.com/support/techsup/journals/fpga_exp/index.htm
Mentor Graphics	http://www.xilinx.com/support/techsup/journals/mentor/index.htm
Cadence	http://www.xilinx.com/support/techsup/journals/cadence/index.htm
Boundary Scan / JTAG	http://www.xilinx.com/support/techsup/journals/jtag/index.htm
CPLD Core tools	http://www.xilinx.com/support/techsup/journals/cpld/index.htm