Moving Towards a Perfect World…

by Carlis Collins,
Managing Editor
of Corporate
Communications,
editor@xilinx.com
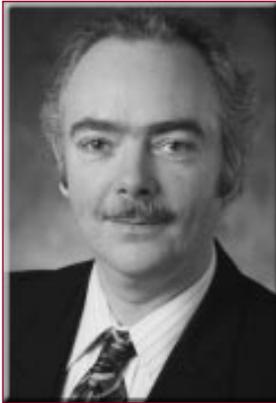
Software is the catalyst that subtly combines your mental creativity with a piece of physical silicon to produce a "living" representation of your thoughts, something that is both physical and non-physical, both matter and energy, heart and spirit. Isn't it a wonder? Perhaps with perfect software, and the perfect device, your thoughts could instantly manifest themselves into real working designs; there would be no limits to your creative potential.

In an imperfect world, the closest you can come to the ideal of instant gratification is through the use of Xilinx FPGAs and development tools. Designs are not instantaneous yet, but with each new generation of Xilinx silicon and software, your design capability increases and your design time decreases.

The version 1.5 release of the Xilinx Alliance Series and Foundation Series software moves you one more step closer to realizing the ideal creative environment. These tools now offer 50% faster compile times and 30% faster clock speeds for average designs, plus they support our new Virtex family, available in Q498, which will offer an unprecedented one million gate density. There has never been anything like this before.

Better software performance is always a good thing, and we are constantly improving our tools with new algorithms and processes. However, as you begin to approach million gate designs you'll need all the software "horsepower" you can get. So, we've added many new performance and productivity enhancing features to our version 1.5 software, smoothing the transition of our FPGAs into ASIC applications.

New AKAspeed Technology

AKAspeed is an array of new algorithms and new algorithmic strategies, combined with advanced new feature sets and applications that are optimized for higher performance, higher density designs. This new software technology, in both the Alliance Series 1.5 and Foundation Series 1.5 software, creates a performance-driven design environment, so you get the industry's highest performance for high-density HDL designs.

AKAspeed includes many new features, plus enhancements to the existing technology such as timing-driven implementation, K-paths, advanced timing analysis algorithms, a robust constraints language, and incremental design capability. This is a powerful and easy to use combination that gives excellent results. AKAspeed includes:

➤ A floorplanner that takes advantage of your knowledge of the structure of your design.

➤ The Xilinx CORE Generator to help you use our rapidly expanding family of cores from Xilinx and our AllianceCORE partners.

➤ A new Graphical Constraints Editor to help you achieve optimal results on the first pass.

➤ Two new design guides for the industry's leading HDL solutions.

➤ The ability to test your design under both best- and worst-case operating conditions.

Your Best HDL Solution

High Level Design Languages, such as VHDL and Verilog, are becoming more attractive as device densities increase. Without these high-level tools, it would be very difficult to design and debug the very large designs that now fit on a single FPGA. Our Alliance Series and Foundation Series software provide an easy-to-use HDL design environment that achieves the highest performance designs.

Though we keep making breakthroughs, there probably is no final "perfect solution," because the problem rapidly evolves. However, Xilinx aggressively pursues in-house development programs, and partnerships with all of the key EDA vendors, to keep you on the leading edge. There is no better way. ◆

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