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HDL VERIFICATION SPECIAL SECTION

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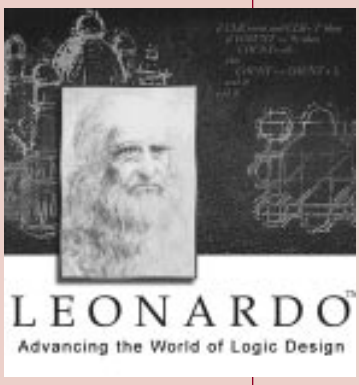
Post-Route Timing Analysis

The Xilinx Alliance Series place and route environment has built-in timing analysis that calculates actual delays for the chip and verifies timing. Leonardo Spectrum can augment the functionality of the Alliance Series software by providing additional functionality such as critical path identification, schematic correlation, and cross highlighting. And because Leonardo Spectrum fully supports backannotation of post-route timing information to the Alliance Series environment, you can take advantage of these features to help verify timing for Xilinx devices.



Leonardo Spectrum is the only FPGA synthesis tool on the market that supports backannotated timing analysis for Xilinx Alliance Series place and route. The Alliance Series environment generates post-routed netlists using "simprims" which are special Xilinx primitives used only for simulation. This "simprims" library is built directly into Leonardo Spectrum along with a netlist interface that reads mapped EDIF netlists and SDF backannotation files, all of which are required for post route static timing analysis.

The Advantages of Backannotated Static Timing Analysis

The advantage of performing post place and route static timing analysis with Leonardo is the timing analysis features available to the user. Some of the more important features are described below:

CRITICAL PATH IDENTIFICATION

The Alliance Series place and route function performs delay analysis on the entire design, presenting all paths to you for viewing via reports. Leonardo Spectrum can perform critical path analysis and report only the timing paths that violate your timing constraints.

CORRELATION TO SCHEMATIC AND HDL SOURCE

Leonardo Spectrum not only has the ability to analyze and report a critical timing path but also to generate a concise schematic fragment showing only the nets and instances of the critical path. This provides a powerful analysis tool for locating timing problems. Using Leonardo Spectrum's backannotated timing interface, critical path schematic fragment viewing is available with the actual post-route timing delays. In addition to generation of critical path fragments, Leonardo Spectrum can also generate fan-in and fan-out fragments from any selected net or instance. For example, clock or reset circuits can be reconstructed from a flip-flop being displayed on the critical path fragment schematic.

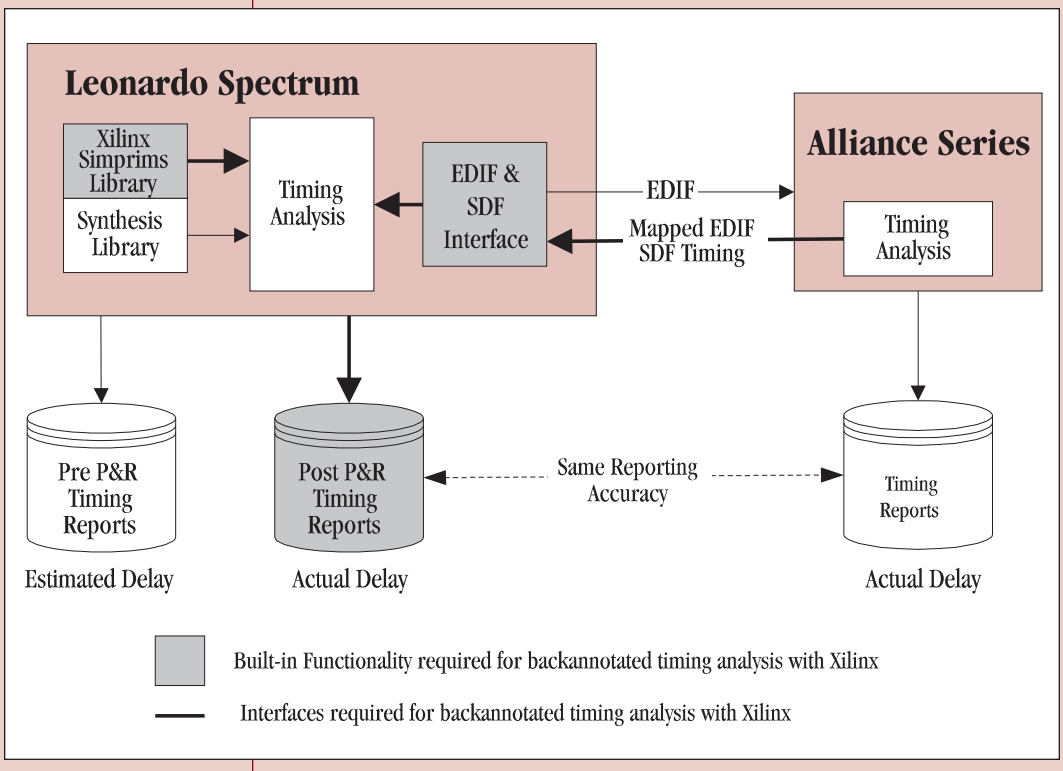
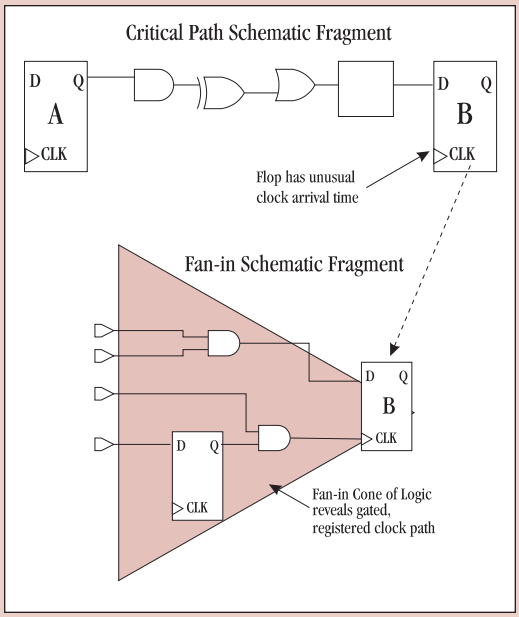


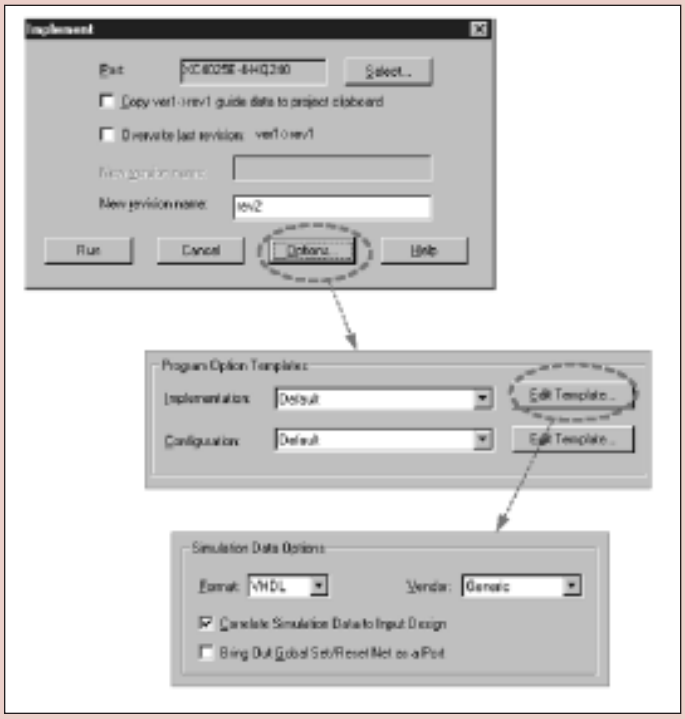
Figure 1 - The Leonardo Spectrum Timing Analysis Environment

with *Leonardo Spectrum*



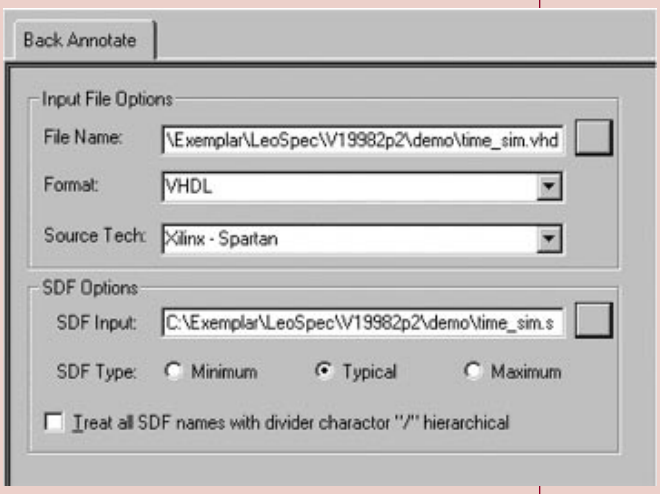
Performing Backannotated Timing Analysis

To perform backannotated static timing analysis with Leonardo Spectrum, the first step is to generate a gate level VHDL or Verilog netlist and an SDF file from the Alliance Series place and route software. To setup the Alliance Series software, perform the following steps:



The Alliance Series place and route software will produce a VHDL file and an SDF backannotation file that can be read into Leonardo Spectrum. Perform the following step to read in. Use Leonardo Spectrum's Back Annotation editor.

And enter in the fields as follows:



At this point you are ready to perform static timing analysis.

Conclusion

Leonardo Spectrum gives you a number of significant advantages when you verify the timing of your designs. ◆