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by David Chiang, Manager, CPLD Technical Marketing, david.chiang@xilinx.com

XC9500XL 3.3V FastFLASH CPLDs

Even More Speed and Features At Lower Costs

m With 10 million 5V XC9500 devices shipped, the world's leading FLASH CPLD family continues to break all records as the fastest growing CPLD family in the industry. Building on that success, we are introducing the new 3.3V XC9500XL. Best

> of all, the XC9500XL family is already supported by your Alliance Series 1.5 development systems.

The XC9500 architecture is already widely recognized as among the most advanced in the world. The new 3.3V XC9500XL improves on

this success with all-new features:

- High-speed FastCONNECT II switch matrix for up to 200MHz system performance
- New ultra-wide block fan-in of 54 for extrawide functions
- Three global clocks with local clock inversion
- Global and individual output enables (OEs) with local OE inversion

Series 1.5 and Foundation

XC9536XL XC9572XL XC95144XL XC95288XL

ű	Macrocells	36	/2	144	288
	Usable Gates	800	1,600	3,200	6,400
ä	Registers	36	72	144	288
	Fastest tPD (ns)	4	5	5	6
	Fastest fSYS (MHz)	200	178	178	151
	Package Options (# user I/O pins)	PC44 (34) VQ64 (36)	PC44 (34) VQ64 (52) TQ100 (72)	TQ100 (81) TQ144 (117)	TQ144 (117) PQ208 (168) BG352 (192)
		CC 10 (2C)	CC 40 (20)	CC1 44 (117)	

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Table 1: XC9500XL CPLD Family

- Dedicated clock-enable signal in each register
- Input hysteresis and bus-hold for all user I/O
- Inputs compatible with 5V, 3.3V, and 2.5V
- Leading-edge 0.35µ feature-size FastFLASH technology

Of course, the XC9500XL architecture also supports the leading-edge features available in the XC9500 family:

- Superior pin-locking characteristics
- Up to 90 product-term functions per macrocell
- Built-in D-type or T-type flip-flop option
- 18-macrocell function blocks for efficient 16-bit look-ahead logic implementations
- Dedicated JTAG/ISP pins for immunity from "ISP Lock-Out"
- Highest programming reliability:10,000 program/erase cycles and 20-year data retention

The XC9500XL devices were developed to operate with leading-edge FPGAs in today's advanced communications and computing systems using a 3.3V power supply. You can optimally partition fast state machines and control functions into XC9500XL devices and partition complex subsystem functions (including cores) into Spartan-XL or XC4000X FPGAs, all using a unified software environment.

Conclusion

Now you have the best 3.3V CPLDs available, fully supported by the Xilinx Alliance Series 1.5 and Foundation Series 1.5 software. The XC9500XL family offers the best in speed, flexibility and reliability, along with the high-quality support you expect from Xilinx. **₹**