The 3.3V SpartanXL™ FPGA Series

Invades New Territory with High Speed and Low Cost

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**84 PLCC, 100K units, -3 speed*

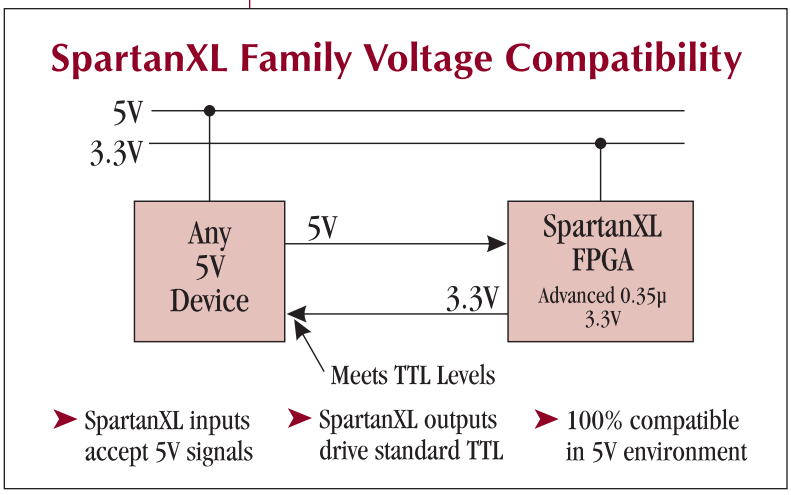
The number of different applications supported by the Spartan™ Series FPGAs has been dramatically increased with the shipment of the new 3.3V SpartanXL family. For the first time, an FPGA family can provide system speeds beyond 100MHz at prices below $3.00*, while supporting all the features needed for complete logic integration. The unique combination of blazing speed and low price eliminates the need for dedicated chips or gate arrays in high-volume applications such as digital imaging and PC peripherals.

Using an advanced 0.35µ process, to achieve smaller die size and higher performance, the SpartanXL family builds on the success of the Spartan Series, the industry's fastest-growing FPGA family. This unique five-layer-metal process, developed by Xilinx, provides the most effective base for a 3.3V logic solution. The five devices in the SpartanXL family offer the same 5,000 to 40,000 gate density range as the 5V Spartan family, introduced in January 1998. Furthermore, they use the same low-cost packages, allowing easy migration between voltage levels.

The SpartanXL architecture features the same synchronous single-port and dual-port SelectRAM memory capabilities offered in the 5V family. The Spartan series is the only ASIC replacement FPGA that offers this key feature. On-chip RAM is useful for scratch-pad memories, shift registers, and FIFOs such as those used in a PCI interface.

The SpartanXL family (and the 5V Spartan family) are the industry's most cost-effective FPGAs, made possible by total cost management, which includes reduction of the assembly and test costs by using low-cost packaging and new, efficient test methodologies.

Figure 1: SpartanXL Family Voltage Compatibility



New Features

The SpartanXL architecture adds several key new features to the original 5V Spartan family. The dedicated carry logic has improved performance, providing 16-bit addition in only 8 ns. Clock routing has been simplified with eight identical, global, low-skew buffers to choose from. The new Express Mode decreases configuration time by a factor of eight. Configuration through the dedicated IEEE-compatible Boundary Scan logic has been simplified, and is now supported by the JTAGProgrammer software and cable. Synthesis is simplified as well, by offering level-sensitive latches throughout the device.

The SpartanXL architecture features the industry's most versatile I/O cell, with features that include:

- 5V input tolerance even before power is applied
- 3.3V or 5V PCI compatibility
- Programmable 12 mA or 24 mA output drive
- Input fast capture latch for shorter setup times
- Output look-up table for the fastest pin-to-pin speeds

High Speed

The SpartanXL series provides system-level speed beyond 100MHz. I/O toggle frequency achieves 100MHz, while functions such as stan-

dard 16-bit binary counters run at 120MHz internally. The SpartanXL speed grades were dramatically improved since the initial software release, and the new speed files are available on WebLINX (www.xilinx.com) in the File Download area.

The 3.3V supply reduces power consumption significantly. Xilinx FPGAs benefit from efficient segmented routing that minimizes the amount of power consumed by each net. For the latest power and speed information, see the SpartanXL Series datasheet on WebLINX.

Software Support and Core Solutions

The SpartanXL family is fully supported by the Xilinx Alliance Series 1.5 and Foundation Series 1.5 development software. New support includes libraries specifically for the Spartan and SpartanXL families, simplifying design with these products. Dozens of Xilinx Alliance partners provide design entry and verification tools.

Pre-defined system functions are available as core solutions for the SpartanXL family. Xilinx offers PCI and DSP LogiCORE solutions via the CORE Generator software, included in the 1.5 version of the Xilinx development system. Several third-party vendors provide AllianceCORE solutions, which are pre-verified for the SpartanXL family. Implementing these common functions in a SpartanXL FPGA costs less than an ASIC, due to the dramatically lower prices offered by the SpartanXL family.

Xilinx Spartan Series

5 Volt (0.5/0.35µ)	XCS05	XCS10	XCS20	XCS30	XCS40
3 Volt (0.35/0.25µ)	XCS05XL	XCS10XL	XCS20XL	XCS30XL	XCS40XL
System Gates	2K-5K	3K-10K	7K-20K	10K-30K	13K-40K
Logic Cells	238	466	950	1368	1862
Max Logic Gates	3,000	5,000	10,000	13,000	20,000
Flip-Flops	360	616	1120	1536	2016
Max RAM bits	3,200	6,272	12,800	18,432	25,088
Max I/O	77	112	160	192	205
Performance	>80MHz	>80MHz	>80MHz	>80MHz	>80MHz

No Compromises:
Performance, RAM, Cores, and Low Price

Figure 2: Availability Chart

Conclusion

The SpartanXL series complements the XC4000XLA family, which applies the same process technology to our higher density devices. For applications where less logic is needed, the XC9500XL family provides the fastest CPLDs in the industry. Together, these families provide the broadest choice of 3.3V devices. Rapid application of aggressive new process technologies allows these PLDs to penetrate new applications that were once the stronghold of ASICs, such as arcade games, graphics cards, and automotive cabin controls.

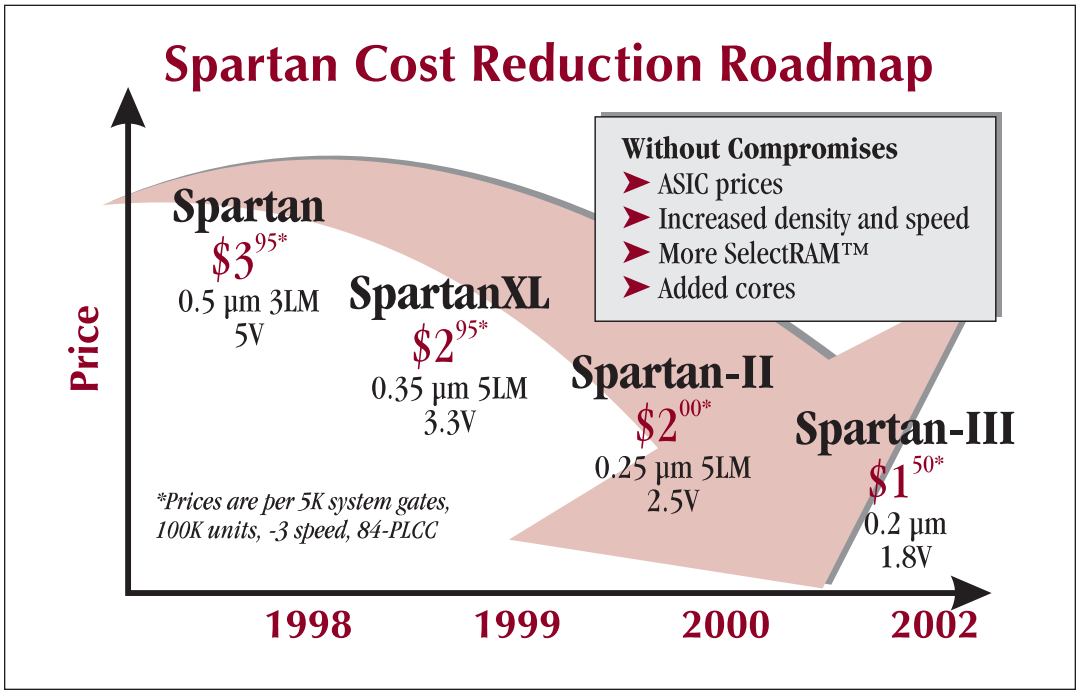


Figure 3: Spartan Cost Reduction Roadmap