New ASIC Estimator –
For Cost Modeling

To help you choose the best development process, Xilinx is now providing, as part of the Silicon Xpresso framework, a new on-line cost modeling tool called the Xilinx ASIC Estimator.

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For many designs it's smart to use FPGAs in volume production, even when the unit cost is higher than ASICs. The time-to-market and ease-of-use advantages of FPGAs often far outweigh the cost advantage that ASICs are traditionally known for. This is proven by a McKinsey study showing that late market entry has a larger effect on profits than development or production cost overruns, especially in very competitive markets.

The Xilinx ASIC Estimator will help you compare various logic development alternatives and decide which to use. The following chart gives some comparisons of the different alternatives:

Comparing Options

	FPGA	Gate Array	Std. Cell
NRE	None	Low-to-Medium	High
Unit Cost	Highest	Low-to-Medium	Lowest
Development time	Lowest	Medium-to-High	Highest
Flexibility	Highest	Low	Lowest

Figure 1

To help you assess the advantages and disadvantages of various production scenarios, the ASIC Estimator allows you to use over 30 different variables to model your project costs and schedule. You can use "what-if" analysis to see how differing NRE costs, unit costs, development time, and production inflexibility can impact overall profitability of the product you are planning or developing.

The ASIC Estimator provides bar charts that show the total cost of using ASICs or FPGAs (**Figure 2**). In addition, a break-even chart shows what unit production volumes are required to justify using an ASIC (**Figure 3**).
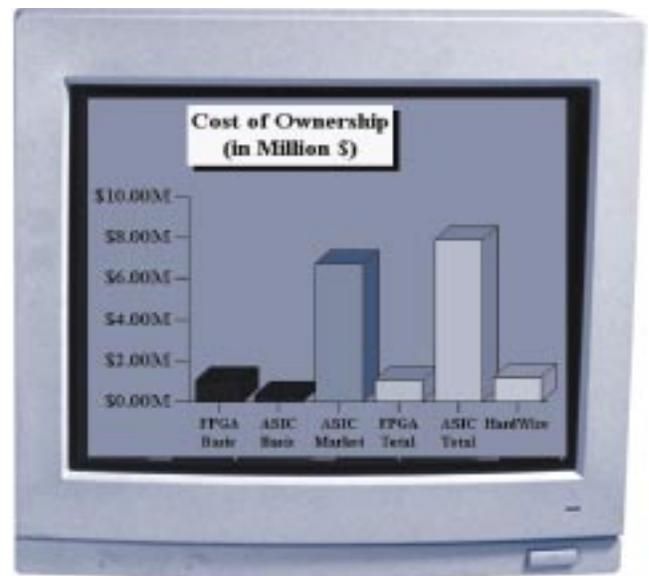
Cost of Ownership
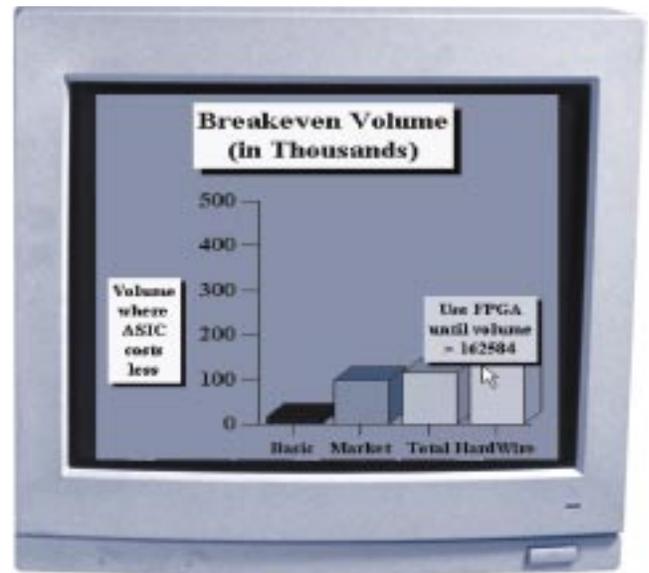

Figure 2

Break-even Bar Chart

Figure 3

Project Timeline

Figure 4

A McKinsey study showed that late market entry has a larger effect on profits than development or production cost overruns, especially in very competitive markets.
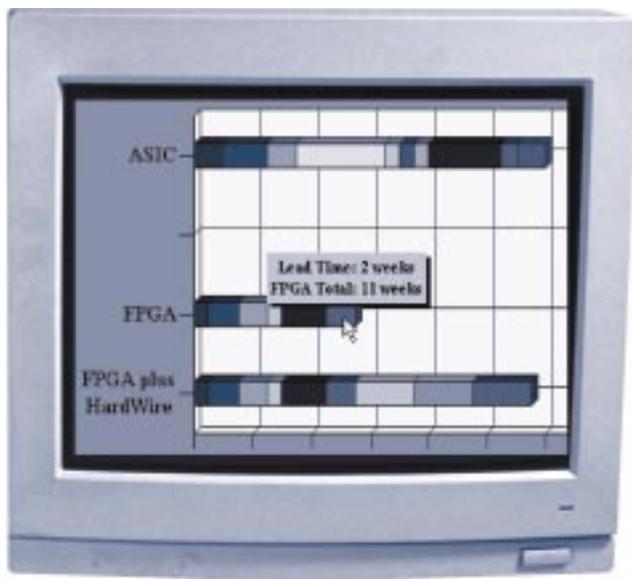
The Advantages of FPGAs

Many companies have a history of using FPGAs only for prototyping and generating proof of concept, eventually converting their designs to ASICs. However, there are often significant delays in the conversion process, and with those delays come the costs of:

- Being late to market and disappointing customers.

- Being late to market and allowing the competition to enter the market first.

- Letting some other company establish a standard based upon their concept.

FPGAs offer a very flexible solution for both prototyping and for early production. With FPGAs, you can design a system, then quickly move to environmental, alpha, beta, and even field tests. You don't have to wait for prototype fabrication and assembly. In addition, you can often be first to market, satisfying customer demands, and establishing a market position. Plus, you can even use the same FPGA design as a platform for the next generation product, often without redesigning your PC board. Using Xilinx Virtex FPGAs for prototype system development and production, you get the fastest time to market compared to gate arrays and standard cell designs (**Figure 4**).

Summary

When you use the Xilinx ASIC Estimator, you will see that it takes a surprisingly large number of units to justify the costs and delays of using ASICs. This has never been more true now that Xilinx has introduced the Virtex product line. **Σ**

You can access the Xilinx ASIC Estimator and our "Cost of Ownership" article (describing the cost models and how the Xilinx ASIC Estimator can help you make the right decision about using ASICs or FPGAs in your next project) at: http://www.xilinx.com/products/hardwire/hardwirehome.htm