XC9500XL CPLDs

Immune to Power Sequencing Problems

With XC9500XL CPLDs you don't need to worry about the possibly damaging effects of improper power supply sequencing. Here's how it works.

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Xilinx XC9500XL CPLDs are designed to operate in either mixed 5V/3.3V systems, 3.3V only systems, or 3.3V/2.5V systems. To handle all conditions, care has been taken to assure that you need not introduce elaborate circuitry to guarantee that any power supplies rise or fall in any particular sequence.

XC9500XL CPLDs are provided with two separate power supply pins. V_{CCINT} supplies power for the internal logic, memory, and charge pumps. V_{CCIO} supplies power for the output drivers that allow the CPLD to be used in either 5V, 3.3V, or 2.5V logic level systems. The Xilinx proprietary ESD circuitry prevents high-voltage damage as well as mixed power system intermingling, as shown in **Figure 1**.

Simplified XC9500XL I/O Cell Structure

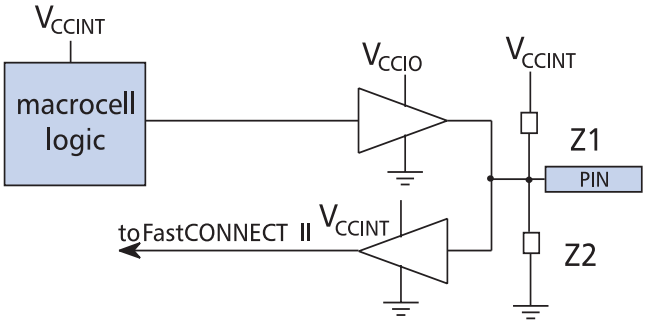

Figure 1

How it Works

Two common power supply configurations occur. First, the single supply system involves attaching both V_{CCINT} and V_{CCIO} to the same voltage, 3.3V +/- 0.3V. The second configuration is where V_{CCINT} is attached to 3.3V and V_{CCIO} is attached to 2.5V. Connecting both supplies to 2.5V is not permitted, neither is connecting V_{CCINT} to 3.3V and V_{CCIO} to 5V (so, we will not consider these two cases). Under these restrictions, it is unlikely that V_{CCIO} and V_{CCINT} will have separate 3.3V supplies, but the following analysis should also cover this case. Of specific interest is the case of having V_{CCIO} = 2.5V and V_{CCINT} = 3.3V.

Specific concern arises if one of the power supplies is off while the other is on. **Figure 2** shows the situation where V_{CCINT} is turned on and V_{CCIO} is turned off. **Figure 3** shows the case where V_{CCINT} is turned off and V_{CCIO} is turned on.

XC9500XL Output Driver with V_{CCIO} Turned Off (Input Receiver not shown)

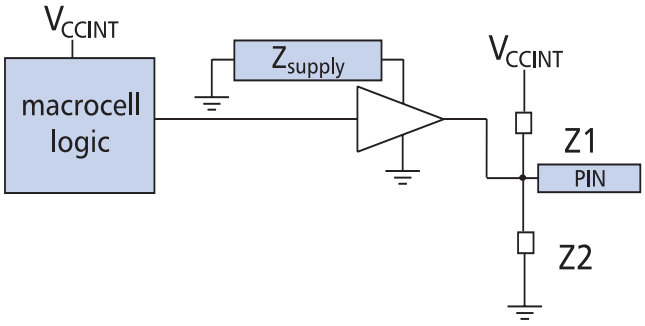

Figure 2

XC9500XL Output Driver with V_{CCIO} Turned On (Input Receiver not shown)

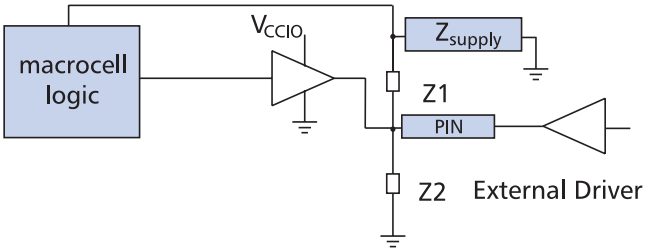

Figure 3

XC9500XL CPLDs are designed to operate in single 3.3V or mixed 3.3V/2.5V/5V systems and tolerate any power supply sequencing applied to them without damaging the CPLD, the supply, or external circuits.

Analyzing the Problem

In analyzing the potential problems, several factors must be considered:

- The supply impedance (Z_{SUPPLY}).
- The current limit of external drivers attached to the pin.
- The state of the macrocell logic driving into the output driver.

We will discuss each factor in order, to see how it affects the condition of the CPLD when power sequencing occurs.

Supply Impedance

For this discussion, we are assuming the power supplies remain attached to the chip pins electrically, whether they are powered up or not. Adding a series switch will physically break the connection, changing the assumptions.

The supply impedance is important because current may flow from the CPLD into the turned off power supply, if a path and an available source (such as the other supply) exists. This can also occur if an external CMOS chip is driving into the CPLD pin (see **Figures 2** and **3**).

Most power supplies have some silicon impedance (the impedance of the attached regulator) and a fairly large capacitor to ground. The supply output capacitor can accept substantial current, but as current arrives, the accumulated charge increases the capacitor voltage. If this turned-off supply is initially uncharged, there may be a substantial initial current. The initial current self-limits as the capacitor voltage approaches the driving voltage (from the pin). This explains how current may initially flow backward into the turned-off power supply. However, as the voltage rises this current becomes negligible.

External Driver Current Limit

Most external CMOS drivers are relatively low current drive devices. Unless a substantially large number of them can deliver a huge current into an XC9500XL pin, the risk of back drive into the pin is very small. The Xilinx proprietary ESD circuitry will limit this to a very low value, so it can usually be ignored.

Macrocell State

Figure 4 shows a simplified model of the output driving structure for an XC9500XL CPLD. If point A is LOW and V_{CCIO} is ON, the pin drives HIGH. If point A is HIGH and V_{CCIO} is ON, the pin drives LOW. If you leave Vccio powered up and V_{CCINT} powered down, static CMOS levels can be delivered to your system. In general, this is harmless.

Close-up of Simplified Output Stage
(ESD circuitry omitted)

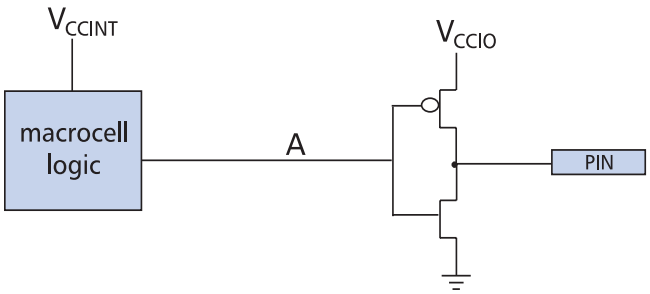

Figure 4

Conclusion

XC9500XL CPLDs are designed to operate in single 3.3V or mixed 3.3V/2.5V/5V systems and tolerate any power supply sequencing applied to them without damaging the CPLD, the supply, or external circuits. Σ